

L NUMBER	HITS	SEARCH TEXT	DB	TIME STAMP
1	305	((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 13:53
2	45	((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 13:11
3	9	(((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6) AND AGILENT	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:08
4	36	(((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6) NOT ((((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6) AND AGILENT)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 13:49
5	33	(((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6) NOT ((((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6) AND AGILENT)) AND DELAY\$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 13:56
6	3	(((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6) NOT ((((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6) AND AGILENT)) NOT ((((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6) NOT ((((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6) AND AGILENT)) AND DELAY\$6)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 13:49
7	274	((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND STROBE\$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 13:55
8	13	(((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND STROBE\$6) AND AGILENT	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 13:53
9	4	(((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND STROBE\$6) AND AGILENT) NOT ((((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND JITTER ) AND STROBE\$6) AND AGILENT)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 13:53
10	333	((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR (OPTICAL ADJ PULSE\$6))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:05
11	272	(((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR (OPTICAL ADJ PULSE\$6))) AND DELAY\$6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 13:56
12	230	(((((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR (OPTICAL ADJ PULSE\$6))) AND DELAY\$6) AND PULSE\$7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 13:56

13	56	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR (OPTICAL ADJ PULSE\$6))) AND DELAY\$6) AND JITTER\$7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:06
14	1391	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTONIC\$6))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:06
15	1430	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:14
16	113	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8)) AND JITTER\$7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:08
17	12	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8)) AND JITTER\$7) AND AGILENT	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:19
18	101	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8)) AND JITTER\$7) NOT (((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8)) AND JITTER\$7) AND AGILENT)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:08
19	1539	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 15:56
21	1044	(MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 16:09
23	292	CONTROL\$9 ADJ JITTER	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:17
24	0	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6)) AND (CONTROL\$9 ADJ JITTER)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 15:21
22	9	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6)) AND ((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:17
25	2	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6)) AND ((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER)) AND AGILENT	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:19
26	7	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6)) AND ((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER)) NOT (((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6)) AND ((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER)) AND AGILENT)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 14:29

28	101	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6)) AND JITTER) NOT (((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6)) AND ((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 15:21
29	10	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6)) AND JITTER) NOT (((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6)) AND ((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER)) NOT (((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8)) AND JITTER\$7) NOT (((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8)) AND JITTER\$7) AND AGILENT))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 15:21
27	110	(((SAMPLERS OR (SAMPLING ADJ CIRCUITS) OR ((FIRST OR SECOND) ADJ (SAMPLER OR (SAMPLING ADJ CIRCUIT)))) ) AND (STROBE\$6 OR OPTICAL\$6 OR PHOTON\$8 OR LASER\$6)) AND JITTER	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 15:26
30	7	(ASSESS\$9) ADJ JITTER	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 15:40
31	1048	((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER) OR ((ASSESS\$9) ADJ JITTER))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 15:51
32	43	(((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER) OR ((ASSESS\$9) ADJ JITTER)) ) AND STROBE\$8	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 15:52
33	101	(((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER) OR ((ASSESS\$9) ADJ JITTER)) ) AND (STROBE\$6 OR ((OPTICAL\$6 OR PHOTON\$8 OR LASER\$6) ADJ PULSE\$7))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 16:06
34	101	(((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER) OR ((ASSESS\$9) ADJ JITTER)) ) AND (STROBE\$6 OR ((OPTICAL\$6 OR PHOTON\$8 OR LASER\$6) ADJ PULSE\$7))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 16:08
35	523	(STROBE\$6 WITH ((GENERAT\$8 OR TRIGGER\$8) ADJ PULSE\$7))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 16:09
36	13	((STROBE\$6 WITH ((GENERAT\$8 OR TRIGGER\$8) ADJ PULSE\$7)) ) AND JITTER	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 16:22
37	2	((STROBE\$6 WITH ((GENERAT\$8 OR TRIGGER\$8) ADJ PULSE\$7)) ) AND (((MEASUR\$9 OR CALCULAT\$9 OR DETERMIN\$9) ADJ JITTER) OR ((ASSESS\$9) ADJ JITTER)) )	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/17 16:22

PAT-NO: JPO2002139553A

DOCUMENT-IDENTIFIER: JP 2002139553 A

TITLE: APPARATUS FOR SPECIFYING END POSITION OF ELECTRONIC  
CIRCUIT ELEMENT AND FOR MEASURING JITTER

PUBN-DATE: MAY 17, 2002

INVENTOR-INFORMATION:

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ASSIGNEE-INFORMATION:

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SCHLUMBERGER TECHNOL INC	N/A

APPL-NO: JP2001252110

APPL-DATE: AUGUST 22, 2001

PRIORITY-DATA: 2000648716 ( AUGUST 25, 2000)

INT-CL (IPC): G01R031/28, G01R029/02, G01R031/319

ABSTRACT:

PROBLEM TO BE SOLVED: To accurately measure a delay in propagation, setup time, and retention time of an electronic circuit element such as IC with an automatic inspection apparatus.

SOLUTION: This apparatus includes a strobe source 10 connected to the control terminal of a pattern source 1 and to the input terminal of a variable clock signal delaying means 12. The strobe source 10 triggers the pattern source so that signals consisting of a series of logic '0' and '1' are output to the input terminal of a device (DUT) 4 to be tested. The DUT 4 propagates this logic series to a flip-flop 6. The signals which have propagated the first and second flip-flops 6 and 8 are corrected after delay. By matching clock signal ends to the flip-flops with data signal ends, the delay time of the DUT is calculated.

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(19) 日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11) 特許出願公開番号  
特開2002-139553  
(P2002-139553A)

(43) 公開日 平成14年 5月17日 (2002.5.17)

(51) Int.Cl. <sup>7</sup>	識別記号	F I	テーマコード* (参考)
G 0 1 R	31/28	G 0 1 R	L 2 G 1 3 2
	29/02		H
	31/319		R

審査請求 未請求 請求項の数27 O L (全 18 頁)

(21) 出願番号 特願2001-252110(P2001-252110)  
(22) 出願日 平成13年 8月22日 (2001.8.22)  
(31) 優先権主張番号 0 9 / 6 4 8 7 1 6  
(32) 優先日 平成12年 8月25日 (2000.8.25)  
(33) 優先権主張国 米国 (U S)

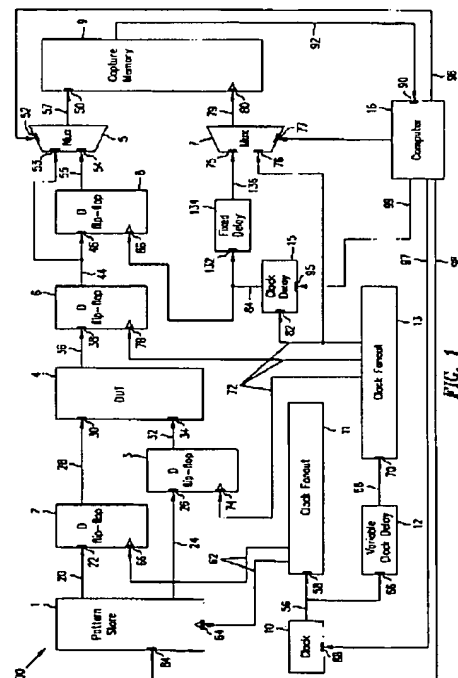
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Fターム(参考) 2G132 AD07 AG02 AG08 AL11

(54) 【発明の名称】 電子回路素子の端部位置特定およびジッタの測定装置

(57) 【要約】 (修正有)

【課題】 自動検査装置による IC など電子回路素子の伝播遅延、セッアップ時間および保留時間の正確な測定。

【解決方法】 この装置は、パターン源 (1) の制御端子および可変クロック信号遅延手段 (12) の入力端子に接続しているストローブ源 (10) を含む。ストローブ源 (10) は、パターン源をトリガして論理「0」および「1」の系列から成る信号を被試験デバイス (DUT) (4) の入力端子に出力させる。DUT (4) は、この論理系列をフリップフロップ (6) に伝播する。第1および第2のフリップフロップ (6), (8) を伝播した信号を遅延の後補足する。フリップフロップへのクロック信号端をデータ信号端と一致させることによって DUT の遅延時間を算出する。



## 【特許請求の範囲】

【請求項1】被検電子回路素子の特性を測定する装置であって、

出力端子を有するストロブ源と、

前記被検電子回路素子の入力端子に接続される出力端子と、前記ストロブ源の前記出力端子に接続した入力端子とを有するパターン源と、

前記ストロブ源の前記出力端子に接続した入力端子と、出力端子とを有する可変遅延手段と、

前記被検電子回路素子の出力端子に接続される入力端子と、前記可変遅延手段の前記出力端子に接続したクロック端子と、出力端子とを有する第1の蓄積素子と、

前記第1の蓄積素子の前記出力端子に接続した入力端子と、前記可変遅延手段の前記出力端子に接続したクロック端子と、出力端子とを有する第2の蓄積素子とを含む測定装置。

【請求項2】前記第2の蓄積素子の前記出力端子に接続した入力端子と、前記可変遅延手段の前記出力端子に接続したクロック端子とを有するメモリをさらに含む請求項1記載の装置。

【請求項3】前記可変遅延手段の前記出力端子と前記第2の蓄積素子の前記クロック端子との間に接続した遅延手段をさらに含む請求項1記載の装置。

【請求項4】前記可変遅延手段の前記出力端子と前記第2の蓄積素子の前記クロック端子との間に接続したゲート手段であって、

前記可変遅延手段の前記出力端子に接続した入力端子と出力端子とを有するカウンタと、

前記カウンタの前記出力端子に接続した第1の入力端子と、前記可変遅延手段の前記出力端子に接続した第2の

入力端子と前記第2の蓄積素子の前記クロック端子に接続した出力端子とを有するANDゲートとを含むゲート手段をさらに含む請求項1記載の装置。

【請求項5】前記第2の蓄積素子の前記出力端子に接続した入力端子と、前記ゲート手段の前記出力端子に接続したクロック端子とを有するメモリをさらに含む請求項4記載の装置。

【請求項6】前記ゲート手段の前記出力端子に接続した入力端子と、前記メモリの前記クロック端子に接続した出力端子とを有する遅延手段をさらに含む請求項5記載の装置。

【請求項7】前記ストロブ源がゲート回路付きのリング発振器を含む請求項1記載の装置。

【請求項8】前記可変遅延手段が、

その可変遅延手段の前記入力端子となる第1の端部と第2の端部とを有する第1の可調整空気誘電体遅延線と、

前記可変遅延手段の前記出力端子となる第1の端部と第2の端部とを有する第2の可調整空気誘電体遅延線と、

前記第1および第2の遅延線の各々の前記第2の端部を結合する結合点と、

前記第1および第2の遅延線の各々の前記第1の端部を取り付けた基板と、

前記第1および第2の遅延線の前記結合した第2の端部を取り付けた直線状位置決め台とを含む請求項1記載の装置。

【請求項9】前記可変遅延手段の前記出力端子を前記被検電子回路素子のクロック端子に接続される請求項1記載の装置。

【請求項10】前記第1の蓄積素子の前記出力端子に接続した入力端子を有するメモリをさらに含む請求項9記載の装置。

【請求項11】前記パターン源の第2の出力端子に接続した入力端子と、前記可変遅延手段の前記出力端子に接続したクロック端子と、前記被検電子回路素子のクロック端子に接続される出力端子とを有する第3の蓄積素子をさらに含む請求項9記載の装置。

【請求項12】前記ストロブ源の入力端子に接続した出力端子を有するコンピュータをさらに含み、それによって前記ストロブ源のストロブ動作の開始および終了を制御する請求項2記載の装置。

【請求項13】前記メモリを前記コンピュータの入力端子に接続した出力端子を有する請求項12記載の装置。

【請求項14】被検電子回路素子の特性を測定する装置であって、

出力端子を有するストロブ源と、

前記被検電子回路素子の入力端子に接続される出力端子と、前記ストロブ源の前記出力端子に接続した入力端子とを有するパターン源と、

前記ストロブ源の前記出力端子に接続した入力端子と、前記被検電子回路素子のクロック端子に接続される

出力端子とを有する可変遅延手段と、

前記被検電子回路素子の出力端子に接続される入力端子と、前記可変遅延手段の前記出力端子に接続したクロック端子と、出力端子とを有する第1の蓄積素子とを含む測定装置。

【請求項15】前記第2の蓄積素子の前記出力端子に接続した入力端子と、前記可変遅延手段の前記出力端子に接続したクロック端子とを有するメモリをさらに含む請求項14記載の装置。

【請求項16】前記パターン源の第2の出力端子に接続した入力端子と、前記可変遅延手段の前記出力端子に接続したクロック端子と、前記被検電子回路素子のクロック端子に接続される出力端子とを有する第2の蓄積素子をさらに含む請求項14記載の装置。

【請求項17】前記ストロブ源がゲート回路付きのリング発振器を含む請求項14記載の装置。

【請求項18】前記可変遅延手段が、

その可変遅延手段の前記入力端子となる第1の端部と第2の端部とを有する第1の可調整空気誘電体遅延線と、

前記可変遅延手段の前記出力端子となる第1の端部と第2の端部とを有する第2の可調整空気誘電体遅延線と、

前記可変遅延手段の前記出力端子となる第1の端部と第2の端部とを有する第2の可調整空気誘電体遅延線と、

2の端部とを有する第2の可調整空気誘電体遅延線と、  
前記第1および第2の遅延線の各々の前記第2の端部を  
結合する結合点と、

前記第1および第2の遅延線の各々の前記第1の端部を  
取り付けた基板と、

前記第1および第2の遅延線の前記結合した第2の端部  
を取り付けた直線状位置決め台とを含む請求項14記載  
の装置。

【請求項19】前記第1の蓄積素子の前記出力端子に接  
続した入力端子と、前記クロック遅延素子の前記出力端  
子に接続したクロック端子と、前記捕捉メモリの前記入  
力端子に接続した出力端子とを有する第2の蓄積素子を  
さらに含む請求項14記載の装置。

【請求項20】前記ストロブ源の入力端子に接続した  
出力端子を有するコンピュータをさらに含み、それによ  
って前記ストロブ源の開始および終了を制御する請求  
項19記載の装置。

【請求項21】前記捕捉メモリを前記コンピュータの入  
力端子に接続した出力端子を有する請求項19記載の装  
置。

【請求項22】被検電子回路素子の特性を測定する方  
法であって、

前記被検電子回路素子に入力信号を第1の時点で供給す  
る過程と、

前記被検電子回路素子の出力信号を前記第1の時点のあ  
との第2の時点で第1の蓄積素子経由で伝搬させる過程  
と、

前記第1の蓄積素子の出力信号を前記第2の時点のあ  
との第3の時点で第2の蓄積素子経由で伝搬させる過程  
と、

前記第2の蓄積素子の前記出力信号を前記第3の時点の  
あとの第4の時点で蓄積する過程とを含む方法。

【請求項23】請求項22記載の前記諸過程を繰り返す  
過程をさらに含む請求項22記載の方法。

【請求項24】前記第1の時点と第2の時点との間の時  
間長を変動させる過程と、請求項22記載の諸過程を繰  
り返す過程とをさらに含む請求項22記載の方法。

【請求項25】被検電子回路素子の特性を測定する方  
法であって、

前記被検電子回路素子に入力信号を第1の時点で供給す  
る過程と、

前記被検電子回路素子を前記第1の時点のあとの第2の  
時点でクロックする過程と、

前記第1の素子の出力信号を前記第2の時点のあとの第  
3の時点で蓄積素子経由で伝搬させる過程と、

前記第1の蓄積素子の前記出力信号を前記第3の時点の  
あとの第4の時点で蓄積する過程とを含む方法。

【請求項26】請求項25記載の前記諸過程を繰り返す  
過程をさらに含む請求項25記載の方法。

【請求項27】前記第1の時点と第2の時点との間の時

間長を変動させる過程と、請求項25記載の諸過程を繰  
り返す過程とをさらに含む請求項25記載の方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は概括的には電子回路  
素子の試験に関し、より詳しくいうと試験対象の電子回  
路素子の伝搬遅延、セットアップ時間および保留時間を  
測定する装置および方法に関する。

【0002】

10 【発明が解決しようとする課題】最新の電子装置および  
それら電子装置の試験システムの設計には電子回路素子  
の伝搬遅延、セットアップ時間および保留時間の正確な  
測定が必要である。信号のタイミングの測定は、ディジ  
タルシステムにおける論理0と論理1とを表す二つの電  
圧レベルの遷移である信号端として信号を特徴づけ、特  
定の位置を基準としてその信号端を位置特定する精度を  
特定することと説明できる。

【0003】半導体集積回路(IC)の特徴把握および  
品質検査可否判定のための自動検査装置は±50ピコ秒  
20 (ps)単位で測定した信号端位置特定精度を仕様書で  
しばしば求められる。それら自動検査システムの信号端  
位置特定精度は、その自動検査システムのタイミング経  
路で多数の互いに異なる回路素子に起因する累積誤差を  
伴う。それら回路素子の特徴把握および可否判定は自動  
検査装置の性能よりもずっと高い精度で行われなければ  
ならない。すなわち、それら回路素子の各々に起因する  
誤差が上記経路で累積されるからである。また、それら  
誤差が構造的なものである場合は、その性質に応じて直  
接に加算される。さらに、それら誤差がランダム雑音に  
30 起因する場合は2乗の和の平方根をとる形で加算され  
る。したがって、自動検査装置のタイミング経路の中の  
回路素子全部によるタイミング誤差の構造的成分および  
ランダム成分を高精度で把握することが、自動検査装置  
の上記信号端位置特定の所要精度を充足するために必要  
である。

【0004】電気信号のタイミング特性の測定装置とし  
ては、リアルタイムオシロスコープ、サンプリングオシ  
ロスコープ、時間間隔測定装置、スペクトル分析器など  
種々の装置がある。それら装置の精度および安定度の測  
定には、高精度の既知の遅延量を有する遅延経路を通  
過した信号を測定する手法が用いられる。これら装置によ  
る測定値を上記遅延経路の既知の長さから導いた遅延量  
と比較する。その遅延経路は例えば同軸信号線で構成す  
る。同軸信号線においては、電気信号の伝搬遅延は、真  
空中の光速に同軸信号線内側導体と外側導体との間の誘  
電体の誘電率の平方根の逆数を乗算した値であることが  
周知である。この誘電体は同軸信号線が剛性の金属であ  
る場合は空気とすることもできる。空気の誘電率は任意  
の温度および湿度について既知である。周知の同軸信号  
50 線の一例としては、U字型接続点で対にした二つの可変



長剛性空気誘電体遅延線、通称「トロンボーン」が挙げられる。

【0005】慣用の高性能オシロスコプの精度は1/2乃至1ピコ秒である。より高精度の自動試験装置に対する需要が高まるに伴って、自動試験装置の構成部分の特徴把握および合否判定に用いられるより高精度の装置に対する需要が高まっている。したがって、自動試験装置の電子回路素子（集積回路や個別部品など）を高精度で特徴把握して合否判定できる装置および方法が必要になっている。

【0006】

【課題を解決するための手段】この発明によると、トランジスタ、集積回路、集積回路配線などの電子回路素子による信号伝搬遅延を比較する装置が得られる。この装置は、パターン源の制御端子および可変クロック信号遅延手段の入力端子に接続した出力線を備えるストロブ源を含む。ストロブ源はパターン源をトリガして論理「0」および「1」の系列から成る信号を被検デバイス（DUT）の入力端子に出力させる。DUTはこの論理「0」および「1」の系列をフリップフロップ（またはそれ以外の蓄積素子）に伝搬する。第1のフリップフロップはDUTからの信号をその第1のフリップフロップが可変クロック信号遅延手段でクロックされる度ごとに第2のフリップフロップ（またはそれ以外の蓄積素子）に伝搬する。第2のフリップフロップは第1のフリップフロップからの信号をクロック信号受信に応答して伝搬する。

【0007】DUTの伝搬遅延の比較のために、パターン源は論理「0」および「1」の同じ系列を各DUTに供給する。クロック信号端を第1のフリップフロップとの間で動かすように可変クロック信号遅延手段を用い、第1のフリップフロップがクロック信号端とデータ信号端（すなわち、DUT出力信号に生ずる一つの論理状態からもう一つの論理状態への遷移）とをほぼ同時に受けるようにする。このタイミング一致はフリップフロップをトリガしてメタ安定状態と呼ばれる短時間の既知の中間状態にする。第2のフリップフロップは第1のフリップフロップの出力信号を蓄積して第1のフリップフロップのメタ安定状態を終了させる。

【0008】第1のフリップフロップがクロック信号端およびデータ信号端をほぼ同時に受けると、第1のフリップフロップの出力信号は、その第1のフリップフロップのセットアップ時間またはホールド時間が確保されなかった場合に第1のフリップフロップの正常伝搬遅延で不安定になる（すなわち、論理「0」と「1」との間で変動する）。クロック信号端とデータ信号端とが正常伝搬遅延で出力信号を予測不可能にするほど接近する時間範囲はメタ安定性領域と呼ばれる。クロック信号端とデータ信号端とが正常伝搬遅延よりもずっと長い時間の経過後に出力信号を予測不可能にするほど接近する範囲は

曖昧領域と呼ばれる。フリップフロップの出力信号の安定に要する通常の伝搬遅延以上の時間を与えればこの曖昧領域は狭くできる。クロック信号端を時間的に第1のフリップフロップに向けて前後に動かすことによって、第2のフリップフロップの記録した第1のフリップフロップの出力信号から曖昧領域（データ信号端を含む）を算定する。したがって、第2のフリップフロップが第1のフリップフロップの正常伝搬時間以上の延長時間（延長遅延）のあと第1のフリップフロップの出力信号を伝搬させればデータ信号端の生起時点を高精度で特定できる。

【0009】一つの実施例では、可変クロック遅延信号で第1のフリップフロップおよび第2のフリップフロップを同時にクロックし、これによって、第1のフリップフロップの出力信号の伝搬にクロック信号繰返し周期一つ分の遅延を第2のフリップフロップが与える。1クロック周期の遅延はデータ信号端の到達時点特定のための短い曖昧領域の形成に必要な延長遅延を与える。同じ入力および同じ延長遅延の下でDUTのための曖昧領域を形成する可変クロック遅延の遅延量を把握したのち、どのDUTの伝搬遅延が最小であるかを判定するようにそれら遅延量を比較する。したがって、この発明の装置および方法は互いに異なるDUTの伝搬遅延を高精度で特性把握し合否判定する。

【0010】また、この発明によるとDUTのセットアップ時間およびホールド時間の比較装置を提供できる。一つの実施例では、可変クロック遅延手段がクロック信号をDUTに供給する。DUTのセットアップ時間およびホールド時間を比較するために、パターン源から論理「0」および「1」の同じ系列を各DUTに供給する。可変クロック遅延手段は、DUTがクロック信号端とデータ信号端（すなわち、DUT入力の一つの論理状態からもう一つの論理状態への遷移）とをほぼ同時に受けるようにクロック信号端を各DUTに向けて前後に動かすのに用いられる。第1のフリップフロップはDUTからの出力の記録に用いられる。

【0011】DUTがクロック信号端をデータ信号端とほぼ同時に受けると、DUTのセットアップ時間およびホールド時間が確保されなかった場合にDUT伝搬遅延では予測不可能になる（すなわち、論理「0」と「1」との間で変動する）。DUTのセットアップ時間は、クロック信号端の到達時点がデータ信号端よりも十分あとでない場合は、不十分である。DUTのホールド時間は、クロック信号端の到達時点がデータ信号端よりも十分に前でない場合は不十分である。したがって、クロック信号端とデータ信号端との時間間隔がDUT出力信号を予測不可能にするほど短くなる時間範囲（曖昧範囲）は、第1のフリップフロップによるDUT出力信号記録時の伝搬遅延でのDUTのセットアップ時間およびホールド時間の和である。クロック信号端を前後に動かすこ

とによって、同じ伝搬遅延での各DUTの曖昧領域は、第1のフリップフロップの記録したDUT出力信号から定まる。

【0012】一つの実施例では、DUTと第1のフリップフロップとを可変クロック遅延手段でクロックし、それによって第1のフリップフロップのDUT出力信号記録時の伝搬遅延に1クロック周期分の遅延を与える。すなわち、各DUTのセットアップ時間およびホールド時間を1クロック周期の伝搬遅延で算定する。DUTの曖昧領域全てをこの伝搬遅延で生ずる可変クロック遅延の遅延量が算定すると、どのDUTのセットアップ時間およびホールド時間が最小であるかを判定するための比較が可能になる。したがって、この発明の装置および方法は、互いに異なるDUTのセットアップ時間およびホールド時間の特性把握および合否判定を高精度で行うことができる。

【0013】

【発明の実施の形態】同一構成要素には全図を通じて同一参照数字を付けて示した図面の図1にこの発明による試験装置100のブロック図を示す。パターン蓄積装置1は信号端によりトリガされるDフリップフロップの入力端子22に接続した出力線20を備える。パターン蓄積装置1は信号端トリガを受けるもう一つのDフリップフロップ3の入力端子26に接続した出力線24を併せ備える。パターン蓄積装置1は、被検デバイス(DUT)4を試験するための論理「0」および「1」のパターン(テストパターン)一つ以上を蓄積している。パターン蓄積装置1はポート84経由で慣用のコンピュータ16からテストパターンを受ける。パターン蓄積装置1は、例えばIllinois州Schaumburg所在のMotorola社製Motorola MC10H145型16×4ビットレジスタファイルで構成する。フリップフロップ2および3は、例えばMotorola MC10EL52型差動データクロックDフリップフロップで構成する。DUT4としては、集積回路、プリント板配線層、固定遅延線、コネクタ、電光変換器ほかの電子部品、すなわち授受信号の伝搬の特性捕捉および合否判定を要する電子部品がある。当業者には明らかなとおり、装置100の機能の制御用に、慣用のコンピュータの代わりにマイクロプロセッサまたはマイクロコントローラを用いることもできる。

【0014】フリップフロップ2はDUT4(装置100の一部ではない)の入力端子30に接続した出力線28を備える。フリップフロップ3はDUT4の入力端子34に接続した出力線32を備える。一つの構成例では、端子34はクロック入力端とする。その構成例では、フリップフロップ2はDUT4への入力(データ)信号を供給し、フリップフロップ3はDUT4へのクロック信号を供給する。DUT4はそのピンに合致するソケット付きの慣用の試験用取付具を通じて装置100に結合する。

【0015】パターン蓄積装置1の出力線20および24はそれぞれの入力端子に直結できる。しかし、テストパターンが複雑になると、パターン蓄積装置1の出力信号タイミングの精度は低下する。したがって、パターン蓄積装置1の出力信号タイミングに追加の制御をかけるようにフリップフロップ2および3を用いる。これらフリップフロップ2および3は、パターン蓄積装置1と同じクロック信号を受けるので、パターン蓄積装置1からの信号を1クロック周期遅延を伴ってDUT4に伝搬させる。

【0016】DUT4は信号端トリガを受けるDフリップフロップ6の入力端子38に接続した出力線36を備える。フリップフロップ6は信号端トリガを受けるDフリップフロップ8の入力端子46およびマルチプレクサ(Mux)5の入力端子53に接続した出力線44を備える。フリップフロップ8はMux5の入力端子に接続した出力線55を備える。Mux5は捕捉メモリ9の入力端子50に接続した出力線57を備える。Mux5は制御端子52を通じてコンピュータ16で制御する。捕捉メモリ9はパターン蓄積装置1と同じ種類のもので構成する。フリップフロップ6および8はフリップフロップ2および3と同じ種類のもので構成する。

【0017】クロック信号源(ストロブ源)10はクロックファンアウト11のクロック端子58および可変クロック遅延素子12のクロック端子66に接続した出力線56を備える。クロック10は慣用のコンピュータ16により制御端子88経由で制御する(例えば、他の構成要素のクロック信号供給の有無の制御)。クロックファンアウト11は、例えばCalifornia州San Diego所在のEdge Semiconductor社製のEdgeE118型クロックファンアウトで構成する。

【0018】図2は可変クロック遅延装置12の構成を示す。この可変クロック遅延装置12は、一方の端部をU字状結合部材206で互いに結合した直線状位置決め台208に取り付けるとともに他方の端部を基板210に取り付けた二つの可調整剛性空気誘電体遅延線202および204を備える(この構成全体がトロンボーンという通称で知られる)。このトロンボーンは、例えばNew Jersey州Livingston所在のMicrofab/FXR社製のST-05SMA型装置で構成できる。直線状位置決め台208は、分解能少なくとも0.02mmのバーニヤ調節機構で調節可能であり、これによってトロンボーン全体の総合遅延量の分解能を少なくとも12フェムト秒としている。

【0019】クロックファンアウト11はパターン蓄積装置1のクロック端子64とフリップフロップ2のクロック端子66とに接続したクロック出力線62を有する。パターン蓄積装置1はクロックされると論理「0」または「1」をフリップフロップ2に出力する。クロック遅延装置はクロックファンアウト11と同種の装置であるクロックファンアウト13のクロック端子70に接

続したクロック出力線68を有する。クロックファンアウト13はフリップフロップ3のクロック端子74、フリップフロップ6のクロック端子78、クロック遅延素子15のクロック端子82およびMux7の入力端子76に接続したクロック出力線72を有する。クロック遅延素子15はフリップフロップ8のクロック端子86および固定遅延素子134の入力端子132に接続したクロック出力線84を有する。固定遅延素子134はMux7の入力端子に接続した出力線136を有する。固定遅延素子は例えば約0.5ナノ秒(例えば長さ3インチ)のプリント板導体線条で構成される。Mux7は制御端子77を通じてコンピュータ90から制御を受ける。

【0020】図3Aは以下クロック遅延素子15-1と呼ぶクロック遅延素子15の構成を示す。クロック遅延素子15-1では、端子82を出力線84に直結する。クロック遅延素子15-1は、フリップフロップ6からフリップフロップ8に伝搬する信号にクロック繰返し周期一つ分の遅延を与えるのにDフリップフロップの動作を利用する。クロック遅延素子15-1を用いる場合はフリップフロップ6および8を同じクロック信号でクロックする。したがって、フリップフロップ6がフリップフロップ8に信号を出力する場合は、フリップフロップ8は次のクロックでクロックされるまでその信号を伝搬させない。

【0021】図3Bは以下クロック遅延素子15-2と呼ぶクロック遅延15のもう一つの構成例を示す。クロック遅延素子15-2は線106経由で端子82に接続した入力端子104を有するANDゲート102を含む。ANDゲート102はプログラマブルカウンタ112の出力線に接続した入力端子108を備える。カウンタ112は線106経由で端子82に接続した入力端子118に受けるクロックパルスの数をカウントする。カウンタ112は、予め設定されたカウントに達すると、線110に活性状態の信号を出力する。ANDゲート102は、端子82からも活性状態の信号を受けると、出力線84に活性状態の信号を出力する。カウンタ112は、バス114経由でポート95に接続したポート116を通じてコンピュータ16により上記所定の値にセットされる。また、コンピュータ16はカウンタ112の現時点のカウントをポート116を通じてリセットする。カウンタ112は例えばMotorola MC10E016型8ビット同期2進アップカウンタで構成できる。

【0022】コンピュータ16は装置100の動作を制御する。コンピュータ16は、Mux7の制御端子77に接続した出力線94と、Mux5の制御端子52に接続した出力線96と、クロック遅延素子15のポート95に接続したバス99と、クロック源10の制御端子88に接続した制御線97と、パターン蓄積装置1のポート84に接続したバス98とに接続した出力線94を有

する。また、コンピュータ16は捕捉メモリ9の記録した出力結果を受けるように捕捉メモリ9のバス92に接続したポート90を備える。一つの構成例では、コンピュータ16は入出力線制御用の入出力信号レジスタカードを備える。入出力信号レジスタカードは、例えばTexas州Austin所在のNational Instrument社製PCI-6601型カードで構成する。

【0023】フリップフロップのメタ安定状態は次式、すなわち

$$TW(TD) = TP * 10 - (\Delta t / \tau)$$

で与えられる。ここでTWは曖昧領域であり、TDは延長遅延であり、TPは正常伝搬遅延であり、 $\Delta t$ は過剰遅延( $TD - TP$ )であり、 $\tau$ はフリップフロップの分解能時定数である。図4はフリップフロップのメタ安定状態で生じた伝搬遅延をクロック入力時点基準のデータ入力時点の関数として示したグラフである。曖昧領域TWは延長遅延TDでフリップフロップの出力信号が予測不可能(「0」と「1」との間で変動する)となるクロック入力時点T0を基準としたデータ入力時点の範囲である。すなわち、延長遅延TDではフリップフロップの出力信号はデータ信号端が範囲TW内のクロック入力時点T0の前か後に到達する場合は予測不可能になる。

【0024】フリップフロップのこれらの特徴を、DUT4のデータ出力時点対応のフリップフロップ6のデータ入力時点(データ信号端)の特定に用いる。装置100の試験するDUT全てに同じ入力信号を加える場合は、DUTの出力信号時点は相対的伝搬遅延に対応する。フリップフロップ6は、遅延線202および204を変動させることにより可変クロック遅延素子12で生じた遅延経路で制御したクロック信号入力(クロック信号端)時点の範囲で各DUTの出力信号を捕捉(伝搬)する。各クロック入力時点のフリップフロップ6の出力を延長遅延TDで繰り返し捕捉する。クロック遅延素子15は、フリップフロップ6の出力信号を延長遅延TDで捕捉メモリ9に伝搬させるように延長遅延TDでフリップフロップ8にクロック信号を送る。捕捉メモリ9はフリップフロップ8の出力信号を記録し、コンピュータ16はコンピュータメモリ9の記録データを読み出す。コンピュータ16は記録データを分析して延長遅延TDの下での曖昧領域、すなわちフリップフロップ6から予測不可能な出力信号を生じさせる少なくとも二つのクロック入力時点(すなわち可変クロック遅延素子12の二つの遅延設定点)の間に位置する曖昧領域の特定のために、蓄積済みデータを分析できる。

【0025】クロック遅延素子15-2を用いた場合は、フリップフロップ8および捕捉メモリ9は、プログラムカウンタが予め定めたカウントに達した後だけクロックする。クロック遅延素子15-2を用いると、フリップフロップ8には出力信号1個だけが記録されるのでメモリ節約となる。

【0026】フリップフロップ8への延長遅延TDはデータ入力時点特定の分解能(データ信号端分解能)を設定する。図4に示すとおり、延長遅延TDをTD1からTD2に増加させると、曖昧領域はTW1からTW2に減少する。上述の実施例は繰返し周期一つ分の延長遅延TDを用いているが、より大きい延長遅延TDもデータ信号端分解能上昇のためにより大きい延長遅延を用いることもできる。しかし、データ信号端分解能は、クロック入力時点調整の分解能(クロック信号端分解能)よりも大きくならないようにする。データ信号端分解能がクロック信号端分解能よりも大きい場合は、出力信号測定値を曖昧領域の片方のデータ入力時点およびもう一方のデータ入力時点に記録することによって省略できる。上述のトロンボーン(図2)はクロック信号端の遅延に高い分解能をもたらし、したがって装置100を用いて高い分解能でデータ信号端の位置を特定できる。

【0027】図5はDUT4への入力信号、DUT4の出力信号(フリップフロップ6への入力信号)、フリップフロップ6への種々のクロック信号およびフリップフロップ8の捕捉したフリップフロップ6の出力信号のタイミング図である。時点T1およびT2においては、クロック信号端120および122は、フリップフロップ6のセットアップ時間およびホールド時間を満たしフリップフロップ6の出力信号が延長遅延TD(クロック1周期)におけるフリップフロップ8による捕捉時に常に論理「1」になるようにデータ信号端130よりも十分に前に到達している。時点T6においては、クロック信号端124はデータ信号端130とほぼ同時に到達し、フリップフロップ6のセットアップ時間またはホールド時間が確保されない。このように、フリップフロップ6の出力信号は延長遅延TDにおけるフリップフロップ8による捕捉時に「1」と「0」との間で変動する(図5においてフリップフロップ6の出力に「?」で表示)。時点T10およびT11においては、クロック信号端126および128はデータ信号端130よりも十分遅れてフリップフロップ6に到達し、フリップフロップ6のセットアップ時間およびホールド時間を満たし、フリップフロップの出力は延長遅延TD2におけるフリップフロップ8による捕捉時に常に論理「0」になる。

【0028】図6は、DUT4について遅延2から遅延10の延長遅延TDで記録した論理「1」の百分比としてフリップフロップ6の出力信号のグラフを示す。一つの構成例では、フリップフロップ6の出力信号を少なくとも100回測定する。遅延2では、フリップフロップ6の出力信号は全部1である。遅延3から6の範囲では、フリップフロップの出力信号は「1」と「0」との組合せであり、論理「1」の百分比は遅延3から遅延6に向かって減少する。遅延10ではフリップフロップ6の出力信号は全部「0」になる。このように、少なくとも遅延2と遅延10との間で延長遅延TDにおいて曖昧

領域が位置特定される。またこれは、DUT4のデータ出力時点、すなわちDUT4の伝搬遅延対応のデータ出力時点が分解能TWで遅延2と遅延4との間で位置特定されることを意味する。上述のとおり、延長遅延TDによってはTWは小さい時間領域であり得る。Motorola MC10EL52型Dフリップフロップで $t_{\text{setup}}$ を200ps、 $t_{\text{hold}}$ を365ps、 $\Delta t$ (TD-TP)を2.5nsとすると、曖昧領域はわずかに約8フェムト秒に留まる。

【0029】一つのDUTについての伝搬遅延を可変クロック遅延素子12(例えば遅延2および遅延10)の二つの遅延設定の間で位置特定すると、もう一つのDUTを同じセットアップで試験して可変クロック遅延素子12の遅延設定を基準とした伝搬遅延の位置特定ができる。第1のDUTの遅延設定が第2の遅延設定よりも短い場合は、第1のDUTの伝搬遅延は第2のDUTのそれよりも短い。このようにしてDUT相互間の相対的伝搬遅延量を算定できる。

【0030】図7は多様なDUTの伝搬遅延を比較する方法140を示す。過程142においてコンピュータ16はテストパターンを蓄積装置1にロードする。オプションの過程144において、コンピュータ16は所定のカウンタをクロック遅延素子15-2にセットする。過程146において、コンピュータ16はMux5をセットしてフリップフロップ8の出力線55を捕捉メモリ9の端子50に接続する。過程148において、コンピュータ16はMux7をセットして固定遅延素子134の線136を捕捉メモリ9の端子80に接続する。過程150において、装置100の操作者は可変クロック遅延素子12の遅延をバーニャ調節機構の手動操作により設定する。代わりに、コンピュータ16で制御するステップモータをこの可変クロック遅延素子12のこのバーニャ調節機構に結合することもできる。

【0031】過程152において、コンピュータ16は上記以外の構成部分にクロック信号をクロック源10から供給させる。過程154において、コンピュータ16は所定時間の経過後、例えば3クロック周期後にそれら構成部分へのクロック信号の供給を終了させる。第1のクロック信号端では、パターン蓄積装置1はテストパターンの論理「1」を出力する。第2のクロック信号端では、Dフリップフロップ2がテストパターンの論理状態をDUT4に出力する。可変クロック遅延素子12の生ずる第2のクロック信号端への遅延のあと、Dフリップフロップ6がDUT4の出力信号を捕捉する。その1クロック周期後(遅延ずみの第3のクロック信号端の時点)にDフリップフロップ8はDフリップフロップ6の出力信号を捕捉する。固定遅延素子134により生じた遅延ずみの第3のクロック信号端への追加の遅延のあと、捕捉メモリ9がDフリップフロップ8の出力を記録する。

【0032】過程156において、コンピュータ16は

捕捉メモリ9から記録済みのデータを読み出す。装置100がクロック遅延素子15-1を用いたクロック遅延素子15が3クロック周期経過後にクロック信号供給を終了するようにコンピュータ16で制御する場合は、捕捉メモリ9で三つの論理状態ひと組、すなわち試験結果である最後の論理状態を含む三つの論理状態ひと組を蓄積する。試験を繰り返す度ごとに捕捉メモリは三つの論理状態の次のひと組を蓄積する。可変クロック遅延素子12の上記遅延設定により試験すべてから得た論理状態組の間の最後の論理の比較によって、その遅延設定が曖昧領域の一点に対応するか否かを判定できる。例えば、二つの論理状態組の間で上記最後の論理状態が変動する場合は、その遅延は図4、5および6に示した曖昧領域の中の点に対応する。クロック遅延素子15-1を用いた場合は、捕捉メモリ9は試験結果だけ（最後のビット）を記録する。クロック遅延素子15-2によって1回だけクロックされるだけだからである。

【0033】過程158において、コンピュータ16（適宜プログラムしてある）は試験のn回目の繰返しが行われるかどうかを判定する。上述のとおり、nは例えば100である。すなわち、可変クロック遅延素子12の遅延設定の各々について、試験を100回繰り返す。現在の繰返しがn以下である場合は、過程158の次にオプションの過程160を行う。または過程158の次に過程162を続ける。オプションの過程160では、コンピュータ16がクロック遅延素子15-2のプログラマブルカウンタの現時点のカウントをリセットする。オプションの過程160のあと過程160を続け、上述の動作過程をn回の繰返し終了まで反復する。

【0034】過程162において、コンピュータ16は曖昧領域を位置特定したか否かを判定する。遅延設定が全部「1」の論理状態（例えば図5の遅延2）の試験結果を生じ、もう一つの論理設定が別の論理状態（例えば図5の遅延10）の試験結果を生じた場合は曖昧領域が位置特定できたことになる。図5に示すとおり、クロック遅延の精度が高いほど曖昧領域の位置特定の精度も高くなる。曖昧領域の位置特定が達成できた場合は、過程162の次に過程164を行い方法140を終了する。または、過程162の次に、可変クロック遅延12のためのもう一つの遅延を設定する過程150を続けて、上述の過程を曖昧領域の位置特定の達成まで反復する。

【0035】装置100のデータ経路の伝搬遅延が既知であれば、DUT4の実際の伝搬遅延を算定できる。DUT4が入力を受ける時点は、クロック源10から線56、クロックファンアウト11、フリップフロップ2および線28経由でDUT4に至るデータ経路の通常の較正によって算定できる。DUT4を曖昧領域の中心に置くクロック信号端をフリップフロップが受ける時点は、クロック源10から線56、可変クロック遅延素子12（メタ安定状態を生ずる遅延量に設定してある）、線6

8、クロックファンアウト13および線72経由でフリップフロップ6に至るデータ経路の較正によって達成できる。DUT4の伝搬遅延はこれら二つの時点の減算によって慣用の較正の精度と同等の精度で算定できる。当業者には明らかなとおり、データ経路の較正は、（1）時間領域反射計測、（2）既知遅延量のDUT（基準ブロック）の挿入、（3）高性能オシロスコープなどの測定装置の利用によって達成できる。

【0036】セットアップ時間とはクロック供給前にデバイスの入力端子でデータが不変のまま留まるべき時間長をいう。ホールド時間とはクロック供給後にデバイス入力端子でデータが不変のまま留まるべき時間長をいう。セットアップ時間およびホールド時間は、そのデバイスが製造業者の特定する伝搬遅延（正常伝搬遅延）で適切な出力信号を生ずるようになるために順守しなければならない。

【0037】セットアップ時間とホールド時間とを測定するために、パターン蓄積装置1およびフリップフロップ2は「0」および「1」から成るテストパターンを生ずる。パターン蓄積装置1はパターン「10」をフリップフロップ2に供給し、DUT4はそのパターンをフリップフロップ2の出力線28から受ける。DUT4はフリップフロップ3の出力線32から端子34に遅延済みのクロック信号も受ける。フリップフロップ3はパターン「01」をパターン蓄積装置1から受けてDUT4へのクロック信号を発生する。フリップフロップ3は可変遅延素子12で遅延を受けたクロック信号でクロックする。クロック信号端をフリップフロップ3とDUT4との間で授受しフリップフロップ2からDUT4へのデータ信号端と同期させるように可変遅延素子12を用いる。フリップフロップ6はDUT4の出力信号を捕捉する。フリップフロップ6とDUT4とは可変遅延素子12で遅延をかけたクロック信号端を共用するので、フリップフロップ6はDUT4の出力信号を1クロック周期のちに捕捉する。このようにしてセットアップ時間およびホールド時間を1クロック周期の伝搬遅延で測定する。

【0038】DUT4がデータ信号端とほぼ同時にクロック信号端を受けると、DUTのセットアップ時間またはホールド時間が確保できなかった場合に伝搬遅延でDUT4の出力信号が予測不可能になる（すなわち、「0」と「1」との間で変動する）。クロック信号端の到来がデータ信号端の到来よりも十分あとでない場合はDUTのセットアップ時間は確保されない。クロック信号端の到来がデータ信号端の到来よりも十分に前でなければDUTのホールド時間は確保されない。このように、DUTの出力信号が予測不可能になる（曖昧領域）ほどにクロック信号端とデータ信号端とが接近する時間範囲はその伝搬遅延におけるDUTのセットアップ時間とホールド時間との和である。クロック信号端を前後に

動かすことによって、同一伝搬遅延における各DUTの曖昧領域が第1のフリップフロップの記録したDUT出力信号から定まる。

【0039】図8はDUT4への入力信号、DUT4への諸クロック信号およびそれら諸クロック信号でクロックされたときのDUT4の出力信号のタイミング図である。時点T12およびT13（可変クロック遅延素子12の遅延12および13にそれぞれ対応）において、それぞれのクロック信号端170および172はデータ信号端179よりも十分に前にフリップフロップ6に到達してDUT4のセットアップ時間およびホールド時間を確保しDUT4の出力信号は1クロック周期の伝搬遅延におけるフリップフロップ6による記録時に常に論理「0」になる。時点T14において、クロック信号端174はデータ信号端179とほぼ同時にDUT4に到達し、セットアップ時間またはホールド時間は確保されない。したがって、DUT4の出力信号は伝搬遅延におけるフリップフロップによる記録時に「1」と「0」との間で変動する（図8においてDUT4の出力の「？」で表示）。時点T15およびT16においては、それぞれのクロック信号端176および178はデータ信号端179よりも十分にあとでDUT4に到達し、DUT4のセットアップ時間およびホールド時間を確保しDUT4の出力信号は延長遅延TD2におけるフリップフロップ6による記録時に常に論理「1」になる。このタイミング図において、セットアップ時間とホールド時間との和は最大でも時点T13とT15との間隔（可変クロック遅延素子12で設定した遅延13および15に対応）である。DUTのセットアップ時間とホールド時間との正確な差は遅延15と遅延13との差である。

【0040】図9はDUTのセットアップ時間とホールド時間との比較の方法180を示す。過程182において、コンピュータ16はテストパターンをパターン蓄積装置1にロードする。過程184において、コンピュータ16はDフリップフロップ6の線44を捕捉メモリ9の端子50に接続するようにMux5をセットする。過程186において、コンピュータ16はクロックファンアウト13の線72を捕捉メモリ9のクロック端子80に接続するようにMux7をセットする。過程188において、検査装置100の操作者がバーニャねじ調節機構を手動操作して可変クロック遅延手段12の遅延量を設定する。代わりに、コンピュータ16で制御するステップモータを可変クロック遅延素子12のバーニャねじ調節機構に結合することもできる。

【0041】過程190において、コンピュータ16は上記以外の構成部分にクロック信号をクロック源10から供給させる。過程192において、コンピュータ16は所定時間の経過後、例えば3クロック周期後にそれら構成部分へのクロック信号の供給を終了させる。第1のクロック信号端では、パターン蓄積装置1はテストパ

ーンの論理「1」を出力する。第2のクロック信号端では、Dフリップフロップ2がテストパターンの論理状態をDUT4に出力する。可変クロック遅延素子12の生ずる第2のクロック信号端への遅延のあと、Dフリップフロップ6がDUT4の出力信号を捕捉する。その1クロック周期後（遅延ずみの第3のクロック信号端の時点）にDフリップフロップ9がDフリップフロップ6の出力信号を捕捉する。

【0042】過程194において、コンピュータ16は捕捉メモリ9から記録ずみのデータを読み出す。捕捉メモリ9はクロック源10でクロックし、捕捉メモリ9で三つの論理状態ひと組、すなわち試験結果である最後の論理状態を含む三つの論理状態ひと組を蓄積する。試験を繰り返す度ごとに捕捉メモリ9は三つの論理状態の次のひと組を蓄積する。可変クロック遅延素子12の上記遅延設定により試験すべてから得た論理状態組の間の最後の論理の比較によって、その遅延設定が1クロック周期の伝搬遅延におけるDUT4の曖昧領域（セットアップ時間とホールド時間との和）の一点に対応するか否かを判定できる。例えば、二つの論理状態組の間で上記最後の論理状態が変動する場合は、その遅延は図8に示した曖昧領域の中の点に対応する。

【0043】過程196において、コンピュータ16は試験のn番目の反復が行われたか否かを判定する。上述のとおり、nは例えば100である。すなわち、可変クロック遅延素子12の各遅延設定で100回の試験を反復する。現時点の反復回数がn以下である場合は過程196のあとに過程190を続け、n回反復の終了まで上述の過程を反復する。その他の場合は過程196のあとに過程198を続ける。

【0044】過程198において、コンピュータ16は曖昧領域を位置特定したか否かを判定する。遅延設定が全部「1」の論理状態（例えば図8の時点T13）の試験結果を生じ、もう一つの論理設定が別の論理状態（例えば図8の時点T16）の試験結果を生じた場合は曖昧領域が位置特定できたことになる。曖昧領域の位置特定が達成できた場合は、過程198の次に過程200を行い方法180を終了する。それ以外の場合は、過程198の次に、可変クロック遅延素子12のためのもう一つの遅延を設定する過程188を続けて、上述の過程を曖昧領域の位置特定の達成まで反復する。

【0045】この発明の実施例と特定の変形とを上述べてきたが、上記以外の変形も可能である。上述のとおり装置100はDUT4の伝搬遅延の高精度校正に用いることができる。したがって、特許請求の範囲の各請求項の真意と範囲を図示の諸変形の説明に限定すべきではない。

【図面の簡単な説明】

【図1】この発明の一つの実施例による検査装置のプロック図。



【図2】

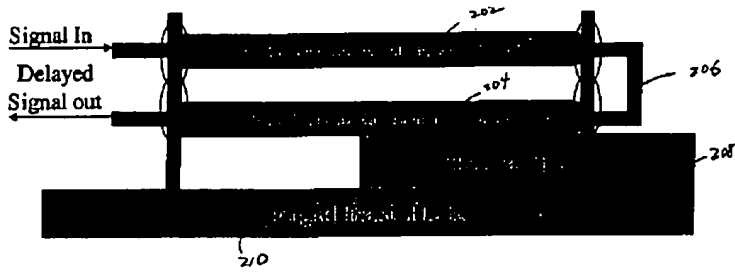


FIG. 2

【図3】

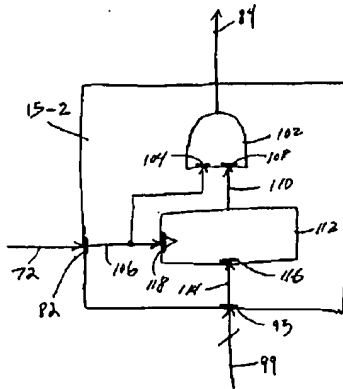


FIG. 3B

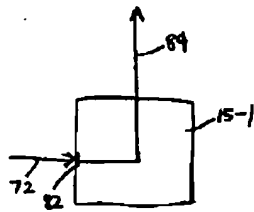


FIG. 3A

【図4】

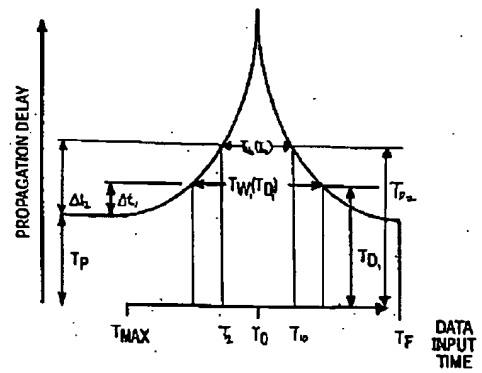


FIG. 4

【図6】

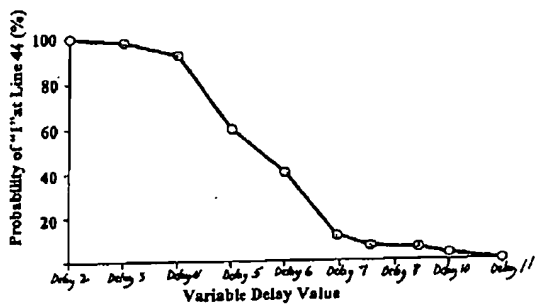
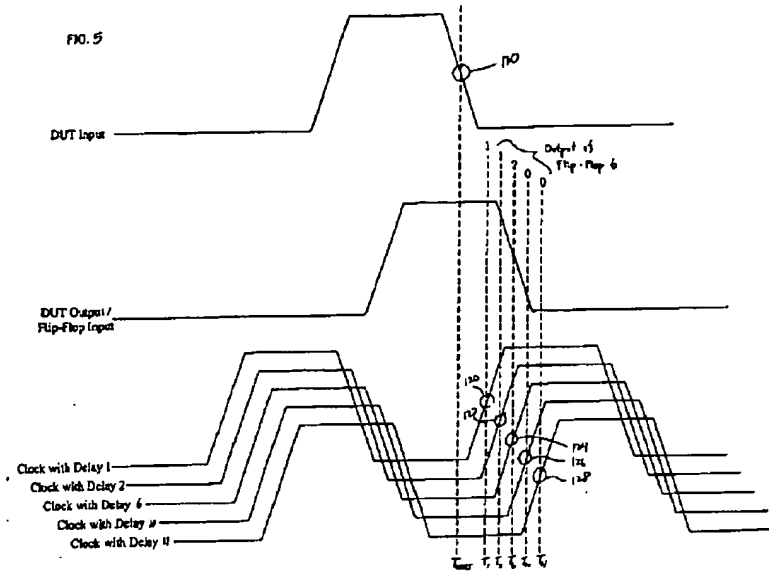


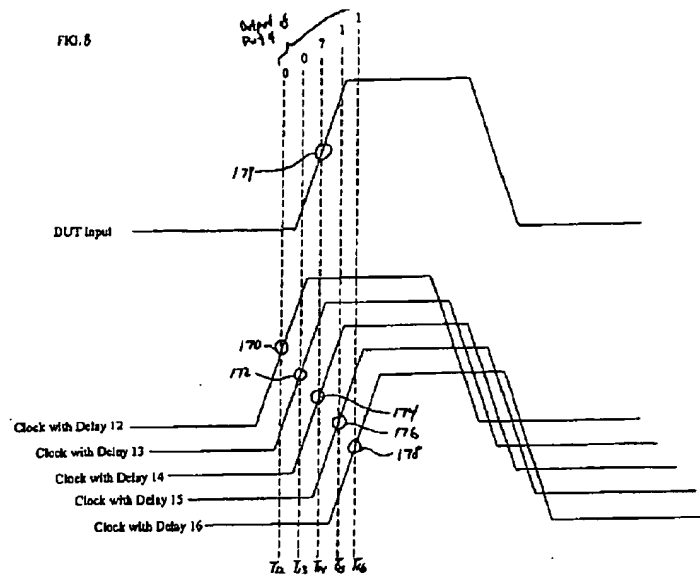
FIG. 6



【図5】



【図8】



【図7】

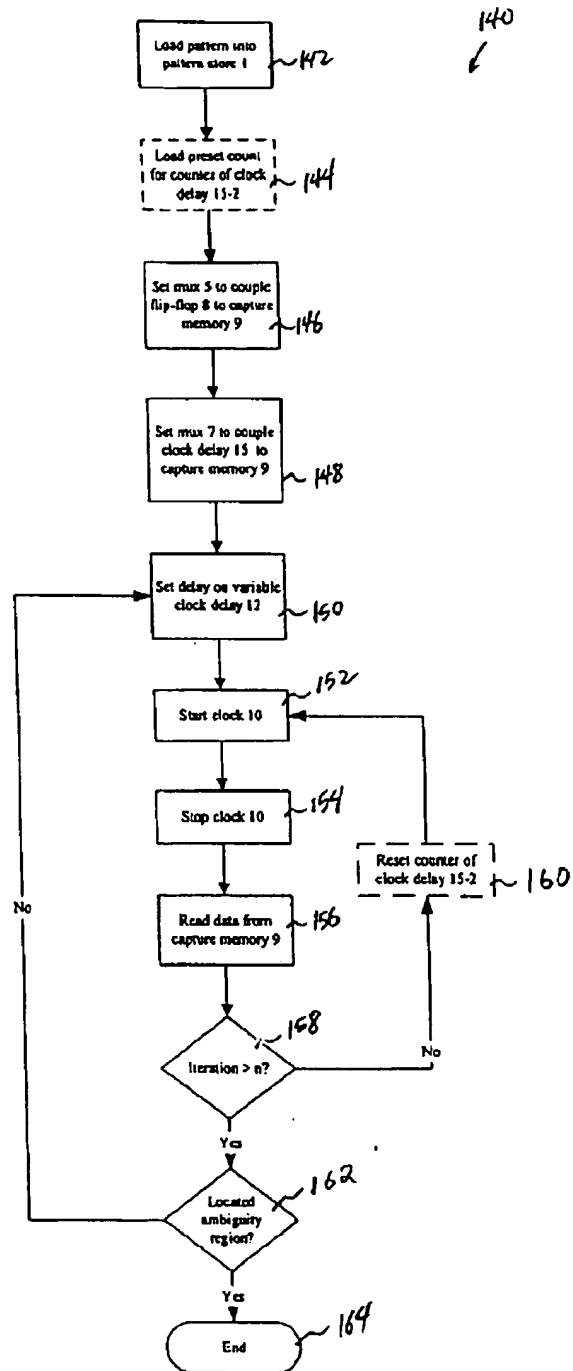


FIG. 7

【図9】

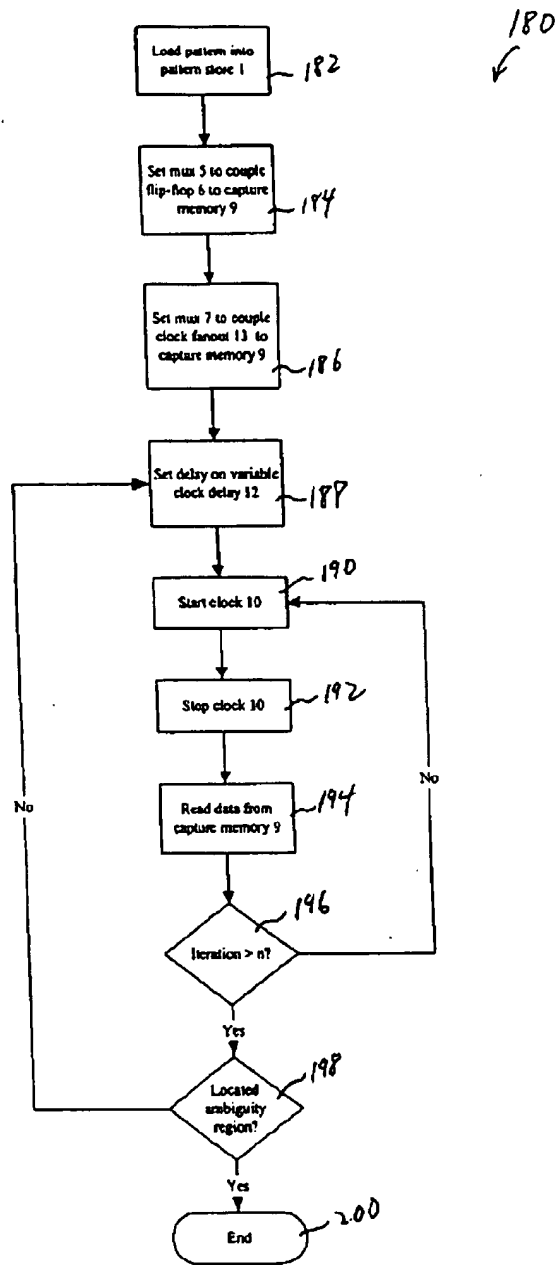


FIG. 9

【手続補正書】

【提出日】平成13年10月26日(2001. 10.

26)

【手続補正1】

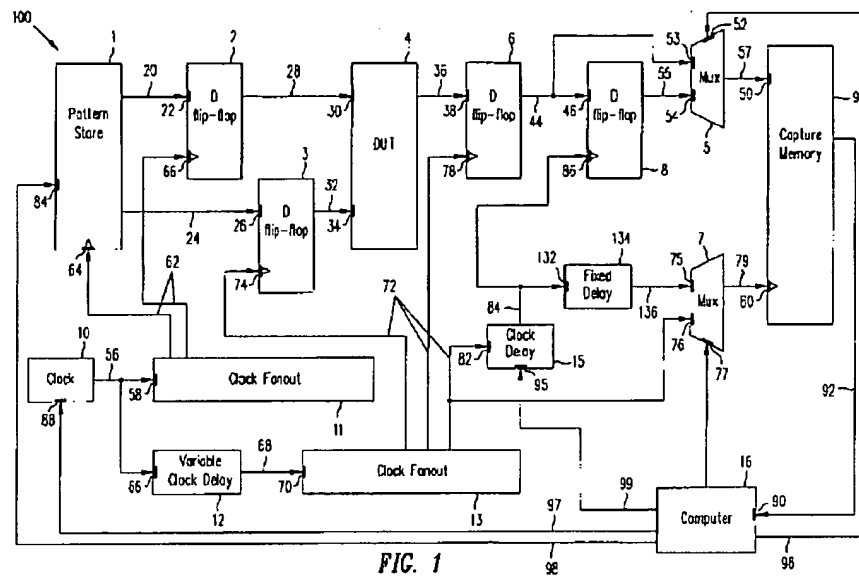
【補正対象書類名】図面

【補正対象項目名】全図

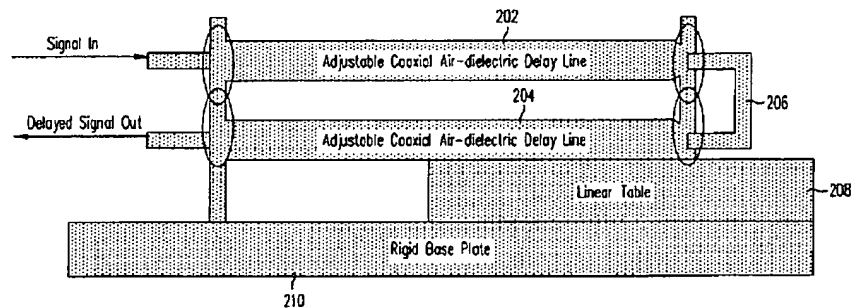
【補正方法】変更

【補正内容】

【図1】



【図2】



【図3】

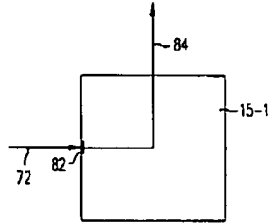


FIG. 3A

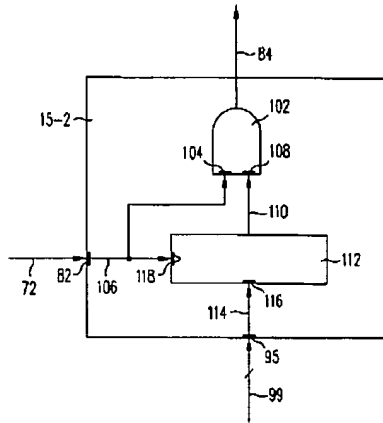


FIG. 3B

【図4】

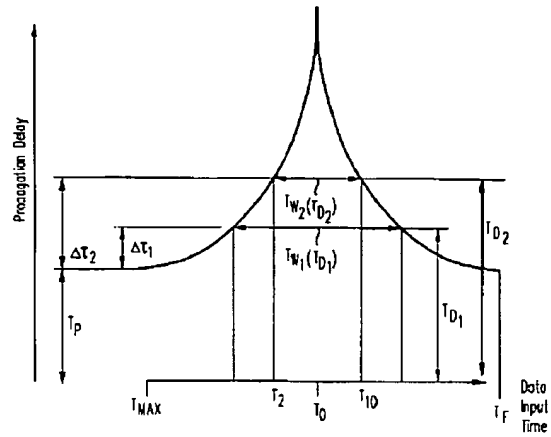


FIG. 4

【図5】

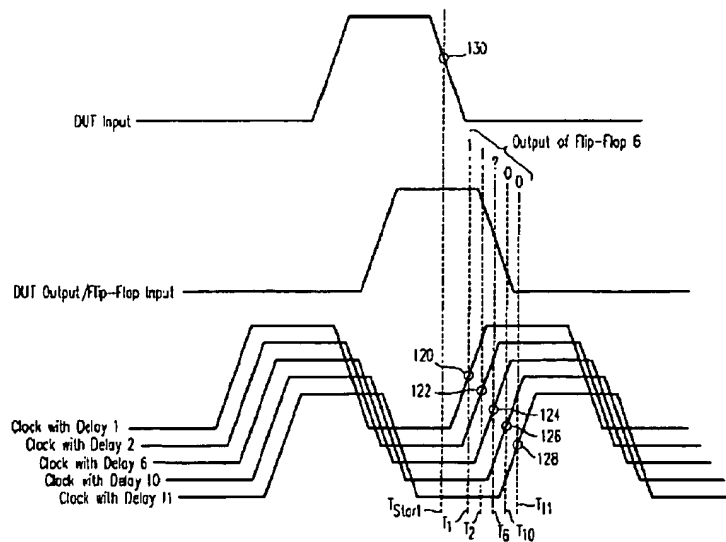


FIG. 5

【図6】

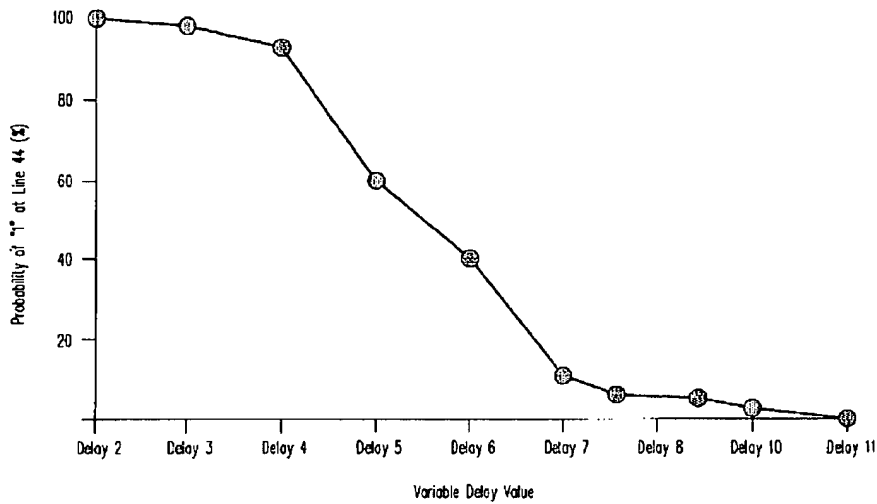


FIG. 6

【図7】

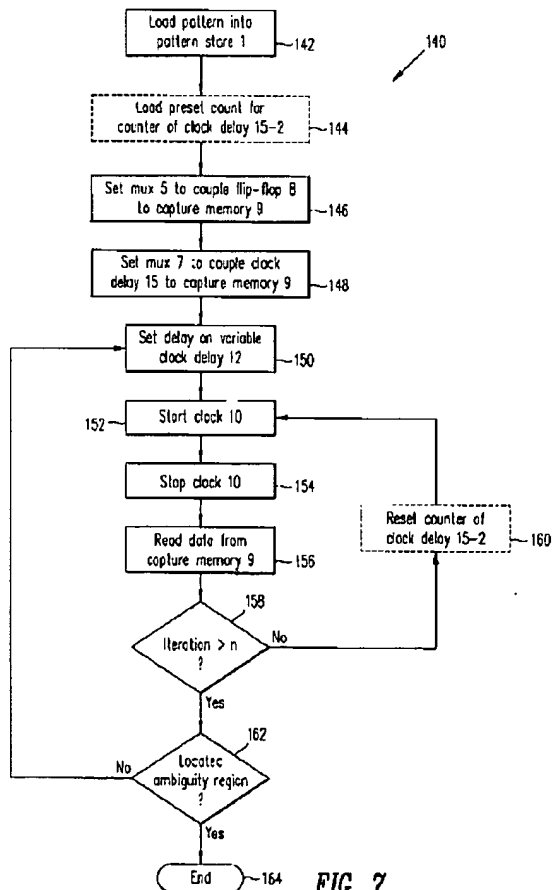


FIG. 7

【図9】

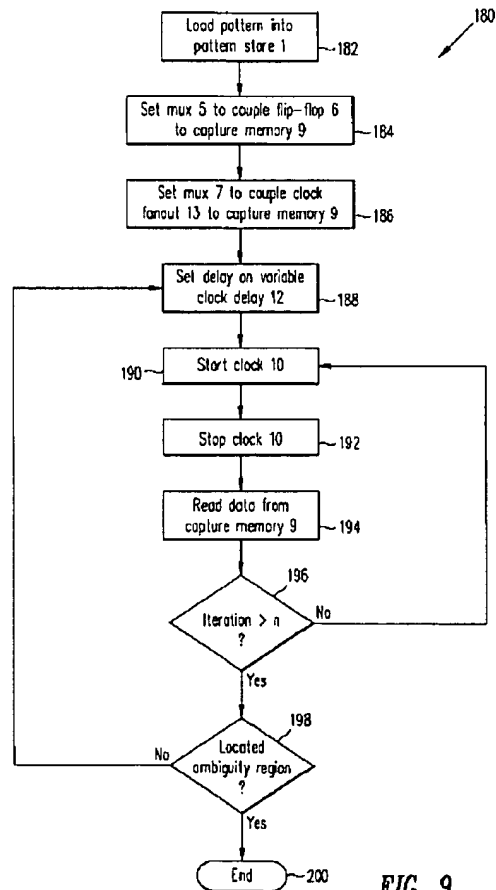


FIG. 9



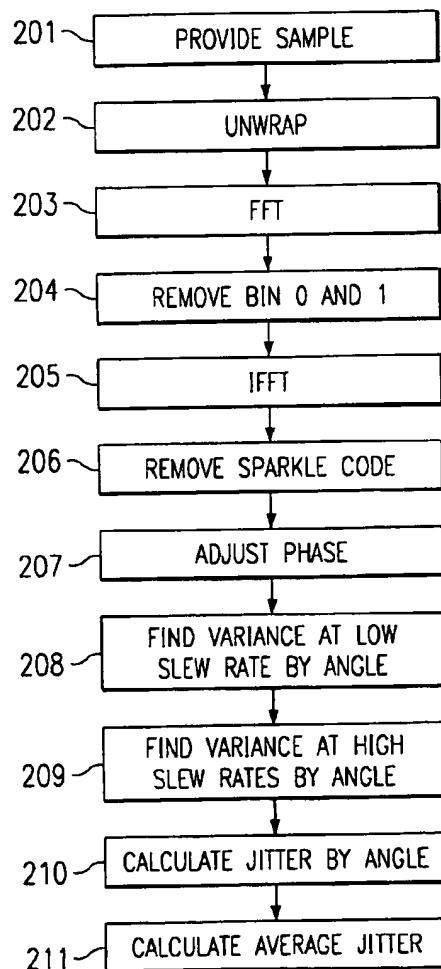
US 20020075951A1

(19) **United States**(12) **Patent Application Publication**  
**Pearson**(10) **Pub. No.: US 2002/0075951 A1**(43) **Pub. Date: Jun. 20, 2002**(54) **METHOD AND APPARATUS TO MEASURE  
JITTER****Publication Classification**(76) **Inventor: Chris C. Pearson, Richardson, TX  
(US)**(51) **Int. Cl.<sup>7</sup> ..... H04B 3/46; H04B 17/00**(52) **U.S. Cl. .... 375/226****Correspondence Address:**  
**TEXAS INSTRUMENTS INCORPORATED**  
**P O BOX 655474, M/S 3999**  
**DALLAS, TX 75265**

(57)

**ABSTRACT**(21) **Appl. No.: 09/974,697**(22) **Filed: Oct. 10, 2001****Related U.S. Application Data**(63) **Non-provisional of provisional application No.  
60/240,830, filed on Oct. 17, 2000.**

A method of determining jitter is provided by providing a sample, performing an unwrap of the data and then performing a Fast Fourier Transform (FFT) of the data. The fundamental is filtered out and an inverse FFT is determined. The sparkle code is taken out and the phase is adjusted to a known phase. The noise difference at both the high and low rates by angles is determined. The jitter by angle is calculated using the high slew variance and low slew variance. The average jitter is then calculated.





US005479120A

**United States Patent** [19]  
**McEwan**

[11] **Patent Number:** **5,479,120**  
[45] **Date of Patent:** **Dec. 26, 1995**

[54] **HIGH SPEED SAMPLER AND  
DEMULTIPLEXER**

[75] Inventor: **Thomas E. McEwan, Livermore, Calif.**

[73] Assignee: **The Regents of the University of  
California, Oakland, Calif.**

[21] Appl. No.: **241,000**

[22] Filed: **May 11, 1994**

**Related U.S. Application Data**

[63] Continuation-in-part of Ser. No. 942,164, Sep. 8, 1992.

[51] Int. Cl.<sup>6</sup> ..... **H03K 5/06**

[52] U.S. Cl. .... **327/91; 327/94**

[58] Field of Search ..... **327/91, 94, 415,  
327/92; 324/76.15**

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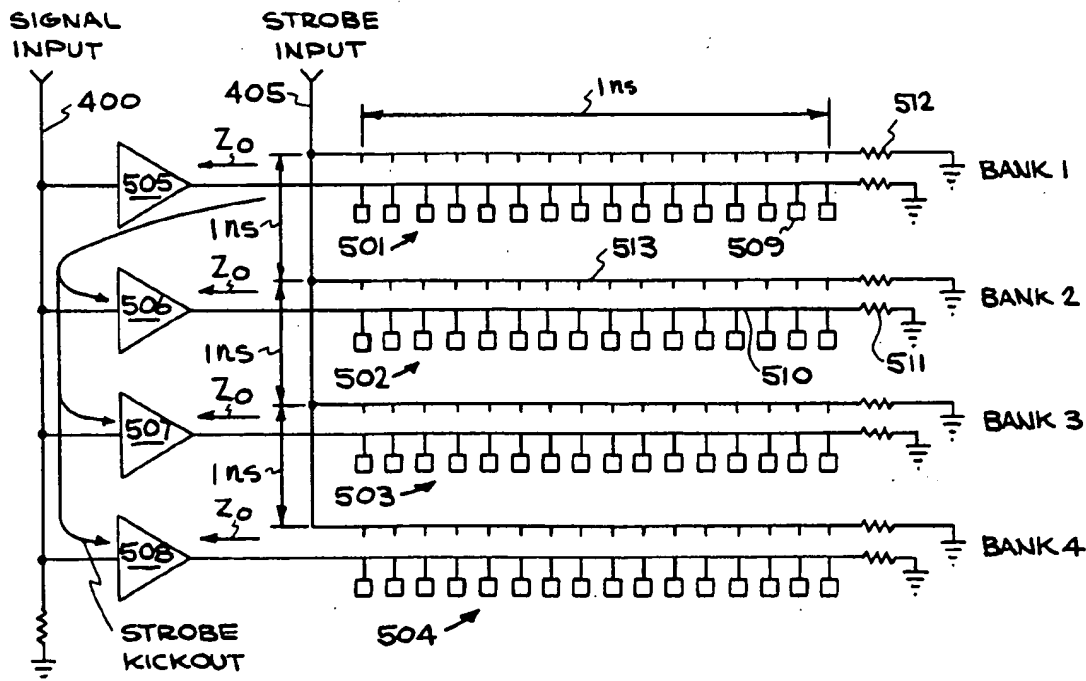
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*Primary Examiner*—Andrew M. Dolinar  
*Attorney, Agent, or Firm*—Henry P. Sartorio

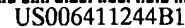
[57] **ABSTRACT**

A high speed sampling demultiplexer based on a plurality of sampler banks, each bank comprising a sample transmission line for transmitting an input signal, a strobe transmission line for transmitting a strobe signal, and a plurality of sampling gates at respective positions along the sample transmission line for sampling the input signal in response to the strobe signal. Strobe control circuitry is coupled to the plurality of banks, and supplies a sequence of bank strobe signals to the strobe transmission lines in each of the plurality of banks, and includes circuits for controlling the timing of the bank strobe signals among the banks of samplers. Input circuitry is included for supplying the input signal to be sampled to the plurality of sample transmission lines in the respective banks. The strobe control circuitry can repetitively strobe the plurality of banks of samplers such that the banks of samplers are cycled to create a long sample length. Second tier demultiplexing circuitry is coupled to each of the samplers in the plurality of banks. The second tier demultiplexing circuitry senses the sample taken by the corresponding sampler each time the bank in which the sampler is found is strobed. A plurality of such samples can be stored by the second tier demultiplexing circuitry for later processing. Repetitive sampling with the high speed transient sampler induces an effect known as "strobe kickout". The sample transmission lines include structures which reduce strobe kickout to acceptable levels, generally 60 dB below the signal, by absorbing the kickout pulses before the next sampling repetition.

**31 Claims, 13 Drawing Sheets**







(10) Patent No.: US 6,411,244 B1  
(45) Date of Patent: Jun. 25, 2002

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*Primary Examiner*—Michael Tokar

*Assistant Examiner*—Lam T. Mai

(74) *Attorney, Agent, or Firm*—William K. Bucher

(57) **ABSTRACT**

(73) Assignee: **Tektronix, Inc., Beaverton, OR (US)**

A phase stable clock circuit includes a phase gate having track-and-hold (T/H) circuits with each T/H circuit receiving a phase shifted continuous sinusoidal signal of predetermined phase and a control input signal to capture and hold phase samples of the sinusoidal signals. In alternative embodiments, a phase correction circuit provides phase correction values that are added to the held phase values to generate corrected phase values and time-error phase lookup table is used to generate time position correction values. The corrected phase values are applied to the phase gate remove deterministic phase errors to generate an output signal with a predetermined startup phase relative to the control input signal transition. The phase error-to-time lookup table adjusts the time placement of waveform record samples after the acquisition of the samples. An optional infinite track-and-hold circuit may be used to generate corrected replica phase values that replace the corrected phase values for longer sample delay periods.

(22) Filed: Mar. 5, 2001

(51) **Int. Cl.<sup>7</sup>** ..... **H03M 1/12**

(52) U.S. Cl. .... 341/155; 341/122; 341/118;  
327/237; 327/306; 327/160; 327/161; 327/162;  
327/165; 302/262; 302/529

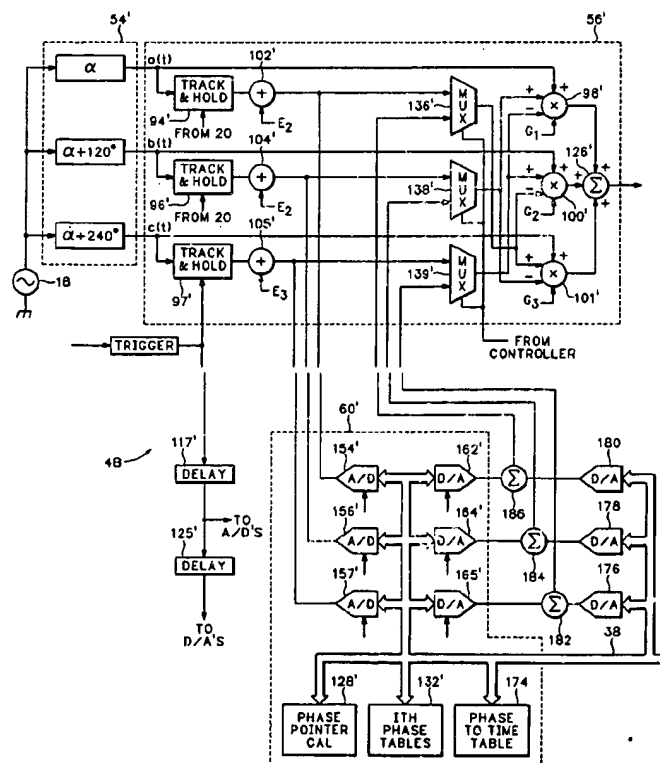
(58) Field of Search ..... 341/155, 122,  
341/118; 327/160, 161, 162, 165, 237,  
356; 307/262, 529

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**28 Claims, 12 Drawing Sheets**





US006384657B1

(12) **United States Patent**  
**Dobos**

(10) Patent No.: **US 6,384,657 B1**

(45) Date of Patent: **May 7, 2002**

(54) **PHASE STARTABLE CLOCK DEVICE  
HAVING IMPROVED STABILITY**

(75) Inventor: **Laszlo Dobos**, Beaverton, OR (US)

(73) Assignee: **Tektronix, Inc.**, Beaverton, OR (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/799,786**

(22) Filed: **Mar. 5, 2001**

(51) Int. Cl.<sup>7</sup> ..... **G06F 1/04**

(52) U.S. Cl. .... **327/294; 327/233**

(58) Field of Search ..... **327/293, 294, 327/299, 171, 129, 231, 298, 291, 233**

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*Primary Examiner*—Kenneth B. Wells

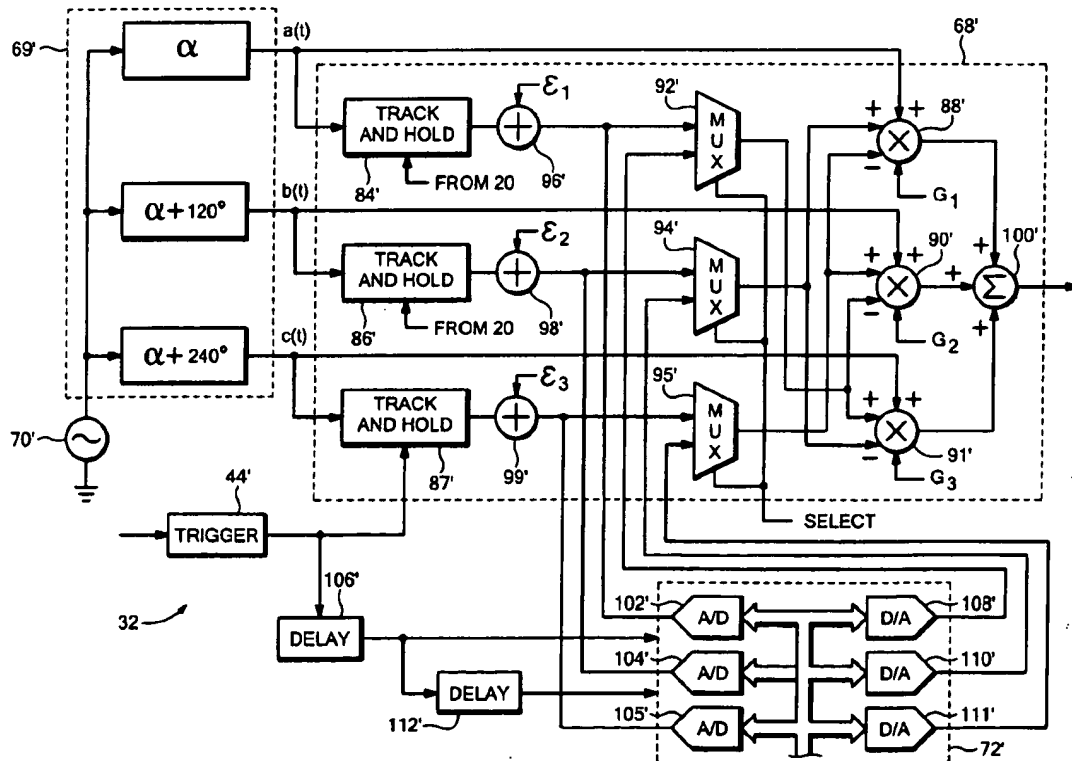
*Assistant Examiner*—Hai L. Nguyen

(74) *Attorney, Agent, or Firm*—William K. Bucher

(57) **ABSTRACT**

A phase stable clock circuit includes a phase gate having track-and-hold (T/H) circuits with each T/H circuit receiving a phase shifted continuous sinusoidal signal of predetermined phase and a control input signal to hold, at a selected time during the signal epoch of the respective sinusoidal signals, phase values of the sinusoidal signals. The respective phase values are coupled to an infinite track-and-hold circuit to generate replicas of the phase values. The phase values and the replica phase values are coupled to respective multiplexers that selectively couple the phase values to multipliers during a first time period and replica phase values during a second time period. The output of each multiplexer is coupled to a multiplier that receives one of the phase shifted continuous sinusoidal signals. The output of the multipliers are summed in a summing circuit to generate an output signal with a predetermined stable startup phase relative to the transition. The use of the infinite track-and-hold improves the long-term stability of the output signal from the summing circuit.

**22 Claims, 4 Drawing Sheets**





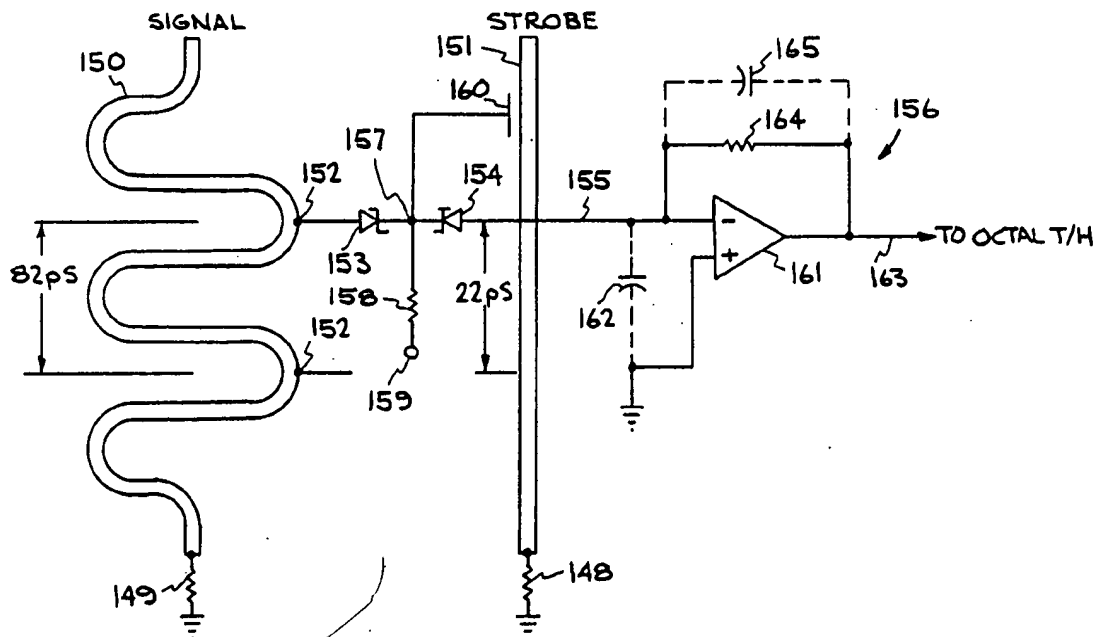
US005519342A

**United States Patent** [19][11] **Patent Number:** 5,519,342**McEwan**[45] **Date of Patent:** May 21, 1996**[54] TRANSIENT DIGITIZER WITH  
DISPLACEMENT CURRENT SAMPLERS**[75] **Inventor:** Thomas E. McEwan, Livermore, Calif.[73] **Assignee:** The Regents of the University of  
California, Oakland, Calif.[21] **Appl. No.:** 240,999[22] **Filed:** May 11, 1994**Related U.S. Application Data**[63] Continuation-in-part of Ser. No. 942,164, Sep. 8, 1992, Pat.  
No. 5,471,162.[51] **Int. Cl.<sup>6</sup>** ..... H03K 5/125[52] **U.S. Cl.** ..... 327/94[58] **Field of Search** ..... 327/91, 94, 92;  
324/76.15**[56] References Cited****U.S. PATENT DOCUMENTS**

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*Primary Examiner—Andrew M. Dolinar*  
*Attorney, Agent, or Firm—Henry P. Sartorio***19 Claims, 13 Drawing Sheets****[57] ABSTRACT**

A low component count, high speed sample gate, and digitizer architecture using the sample gates is based on use of a signal transmission line, a strobe transmission line and a plurality of sample gates connected to the sample transmission line at a plurality of positions. The sample gates include a strobe pickoff structure near the strobe transmission line which generates a charge displacement current in response to propagation of the strobe signal on the strobe transmission line sufficient to trigger the sample gate. The sample gate comprises a two-diode sampling bridge and is connected to a meandered signal transmission line at one end and to a charge-holding cap at the other. The common cathodes are reverse biased. A voltage step is propagated down the strobe transmission line. As the step propagates past a capacitive pickoff, displacement current  $i=c(dv/dt)$ , flows into the cathodes, driving the bridge into conduction and thereby charging the charge-holding capacitor to a value related to the signal. A charge amplifier converts the charge on the charge-holding capacitor to an output voltage. The sampler is mounted on a printed circuit board, and the sample transmission line and strobe transmission line comprise coplanar microstrips formed on a surface of the substrate. Also, the strobe pickoff structure may comprise a planar pad adjacent the strobe transmission line on the printed circuit board.





US006549572B1

(12) **United States Patent**  
**Anderson et al.**

(10) **Patent No.:** **US 6,549,572 B1**  
(45) **Date of Patent:** **Apr. 15, 2003**

(54) **METHOD AND APPARATUS FOR  
AUTOMATED TIME DOMAIN MONITORING  
IN OPTICAL NETWORKS**

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(\*) **Notice:** Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** **09/304,274**

(22) **Filed:** **May 6, 1999**

**Related U.S. Application Data**

(60) Provisional application No. 60/085,347, filed on May 13,  
1998.

(51) **Int. Cl.<sup>7</sup>** ..... **H04B 17/00**

(52) **U.S. Cl.** ..... **375/225**

(58) **Field of Search** ..... **375/376, 354,**  
**375/360, 361, 225, 294; 356/73.1; 702/79**

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*Primary Examiner*—Stephen Chin

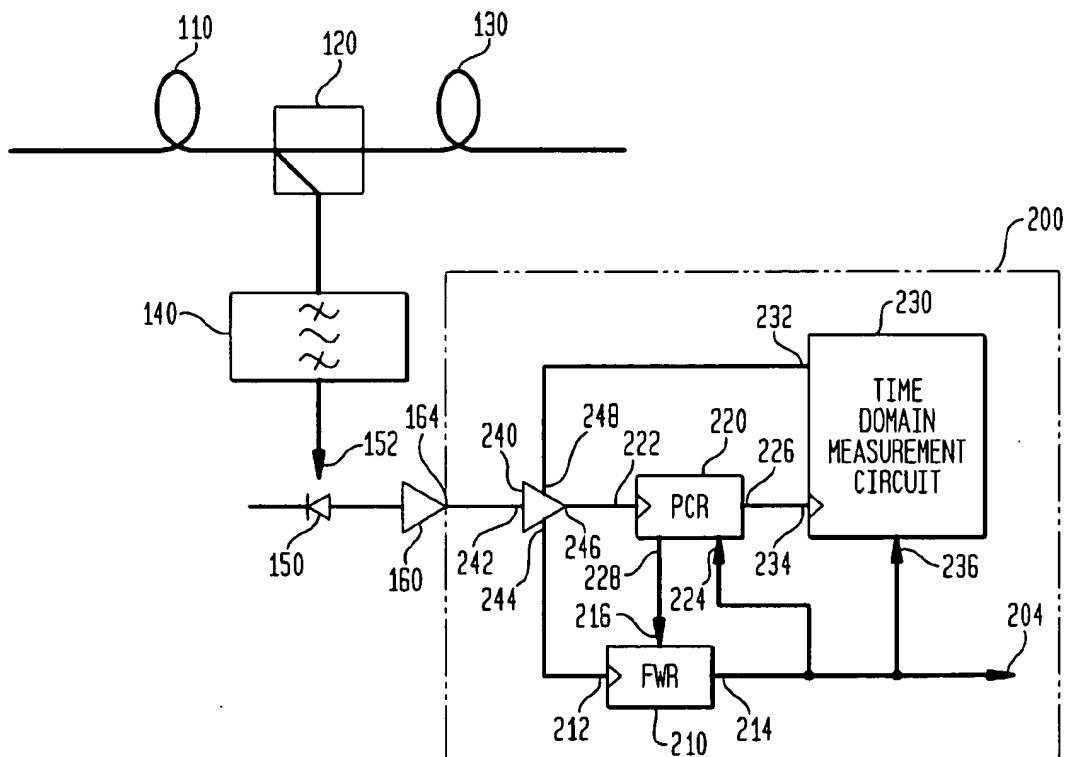
*Assistant Examiner*—Kevin Kim

(74) *Attorney, Agent, or Firm*—Joseph Giordano; James W.  
Falk

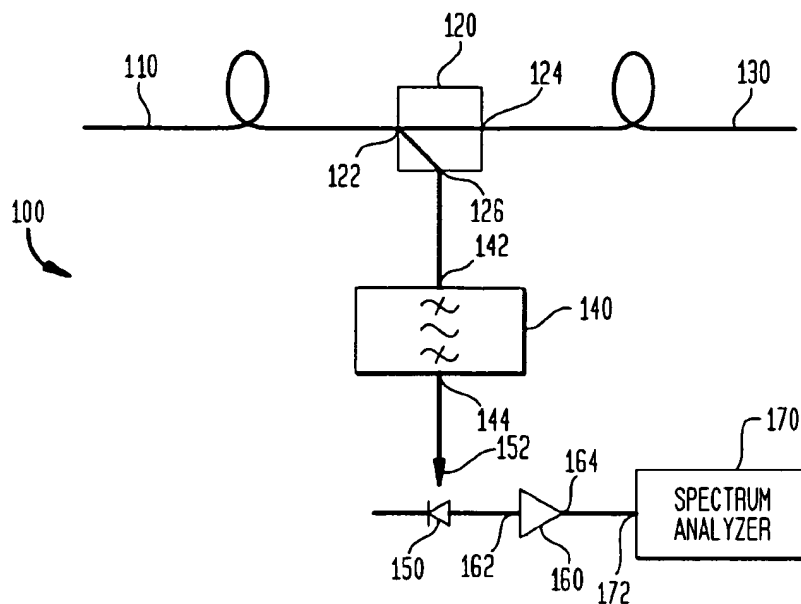
(57) **ABSTRACT**

Methods and apparatuses are provided for determining characteristics of an input optical signal in an optical network. An optical signal monitoring apparatus estimates a minimum time interval between transitions in the input signal, determines a clock signal based on the estimated minimum time interval, and performs a time domain measurement on the input signal based on the determined clock signal. The optical signal monitoring apparatus samples the input signal based on the determined clock signal and determines the characteristics of the input signal.

**41 Claims, 6 Drawing Sheets**



**FIG. 1**  
(PRIOR ART)



**FIG. 2**

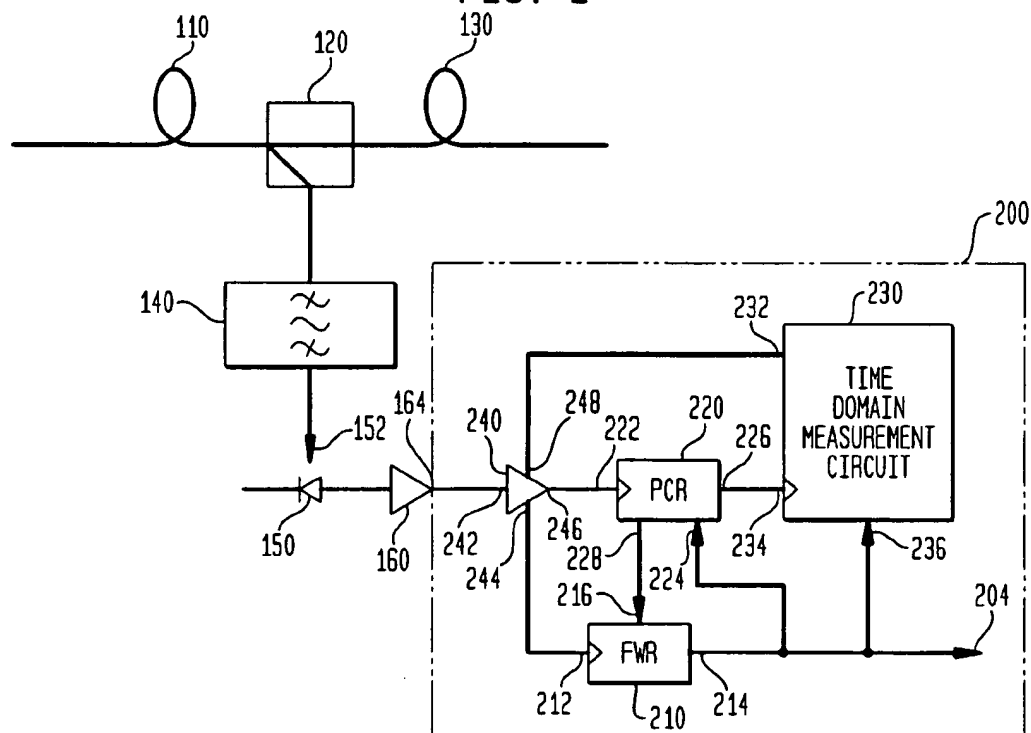
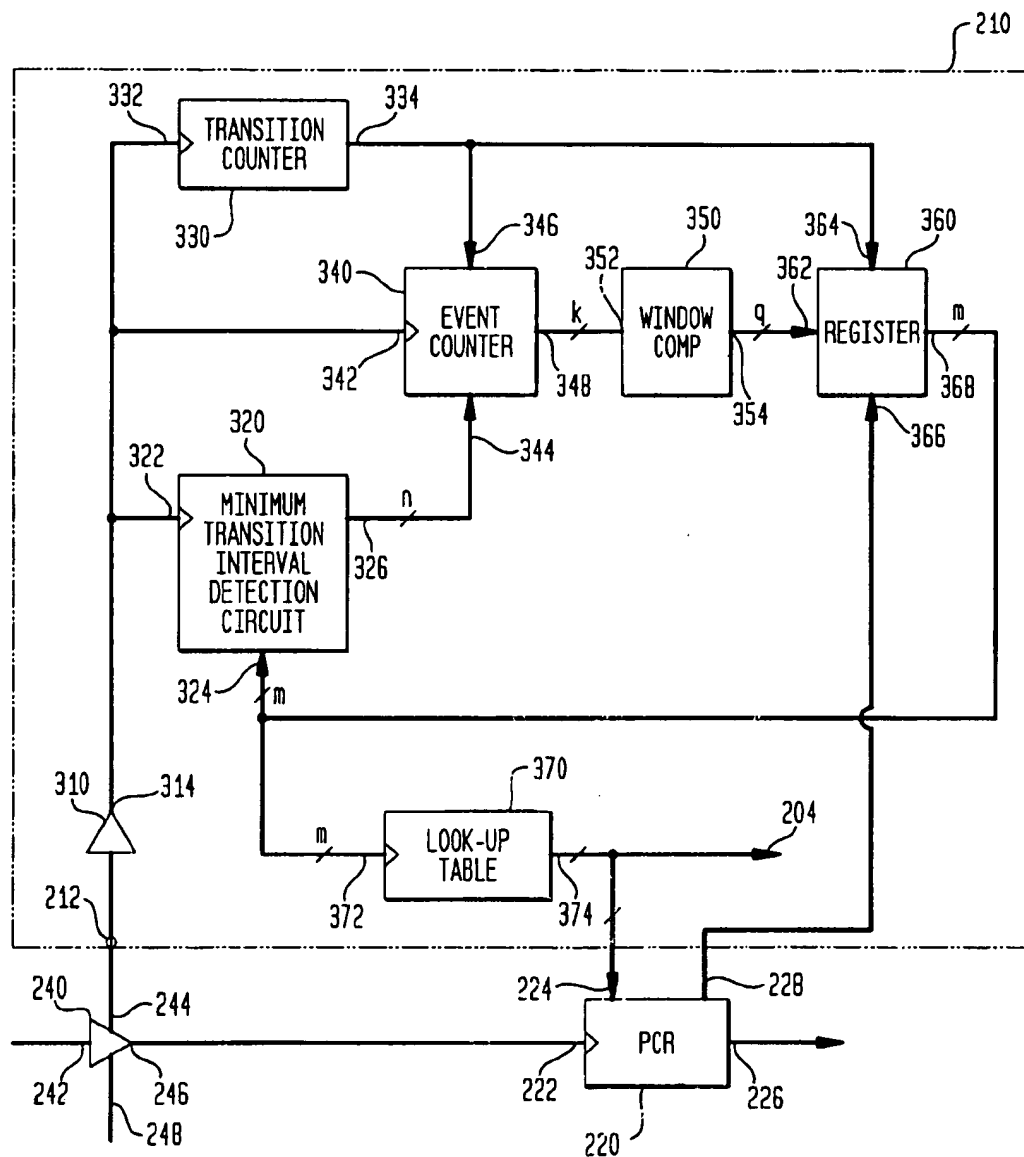


FIG. 3



**FIG. 4**

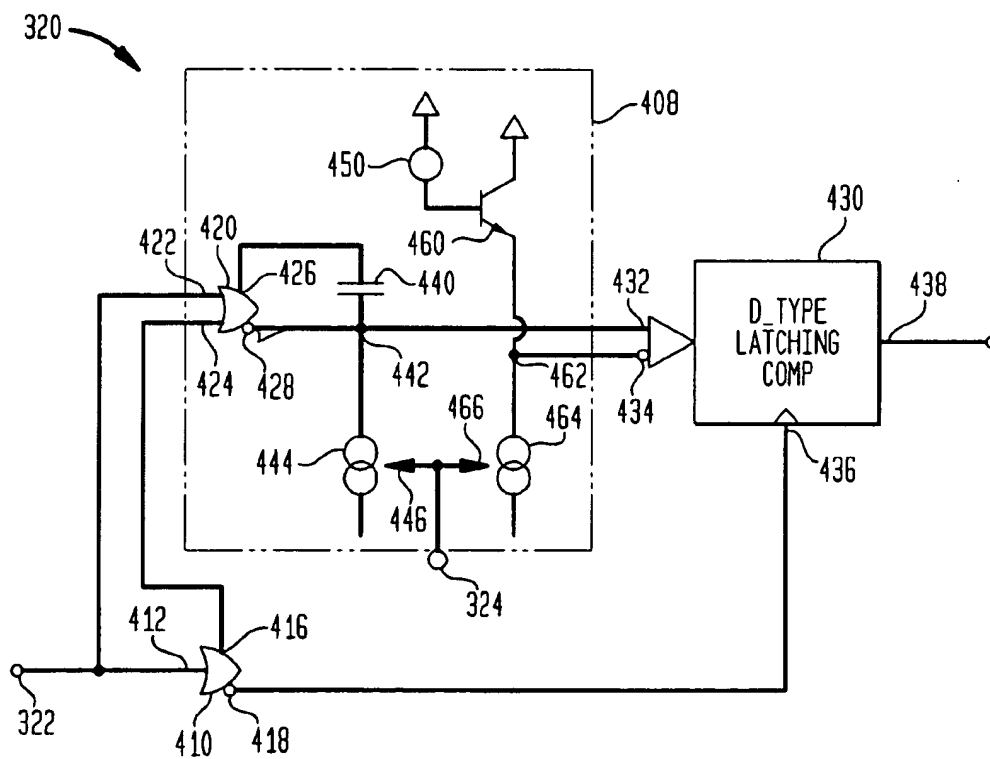


FIG. 5A

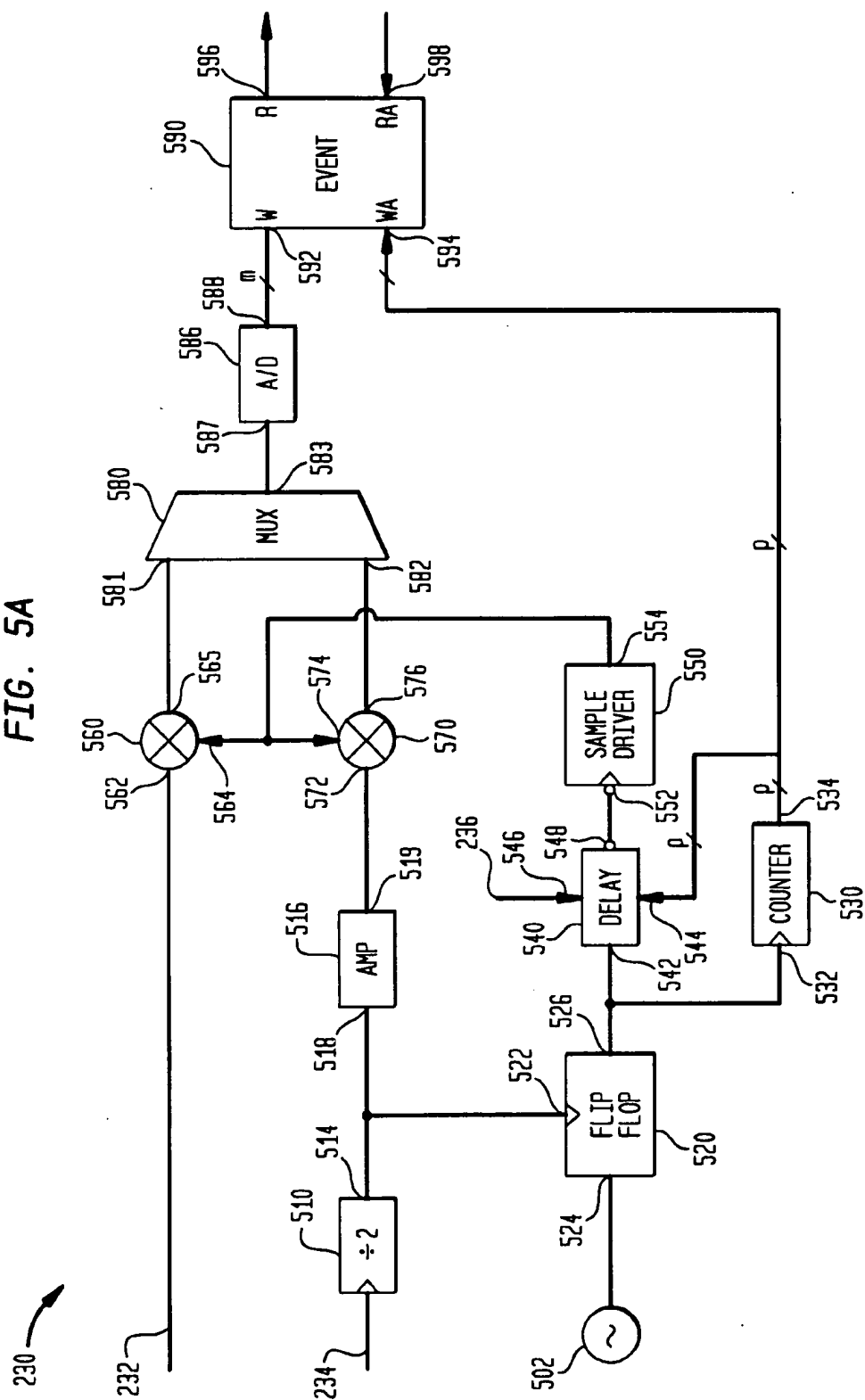




FIG. 5B

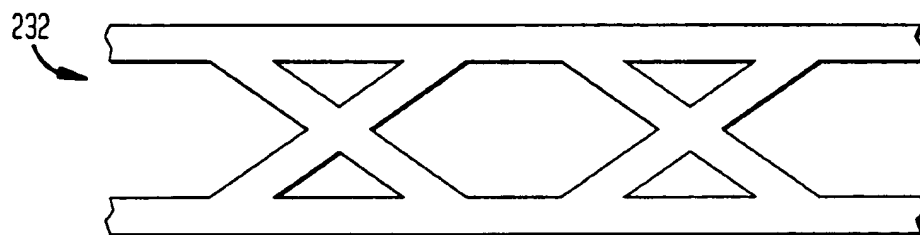


FIG. 5C

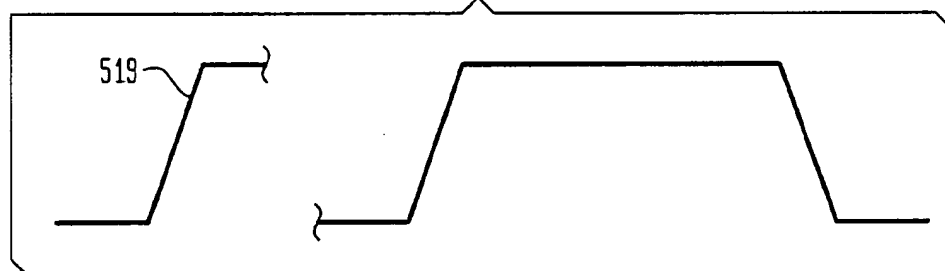
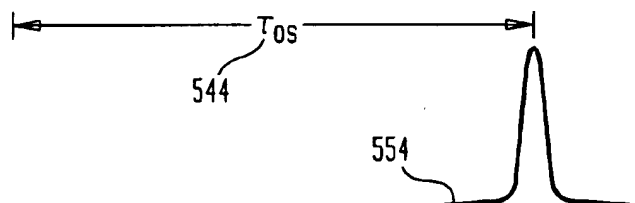
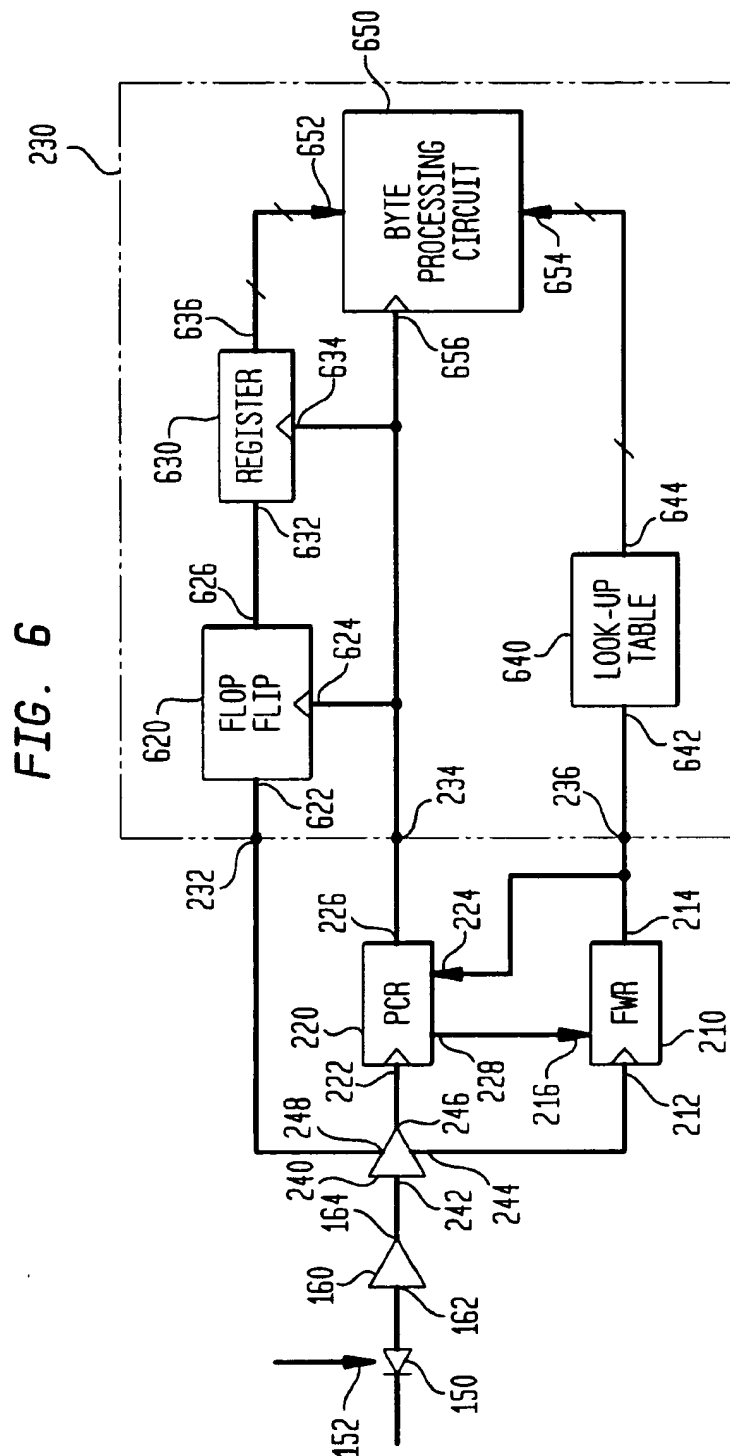


FIG. 5D





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# METHOD AND APPARATUS FOR AUTOMATED TIME DOMAIN MONITORING IN OPTICAL NETWORKS

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 60/085,347, filed May 13, 1998, the contents of which are incorporated herein by reference. This application is also related to U.S. application Ser. No. 09/199,480, entitled "Method and Apparatus for Variable Bit Rate Clock Recovery", filed Nov. 25, 1998, and now U.S. Pat. No. 6,285,722, Sep. 4, 2001, the contents of which are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

The present invention relates generally to optical networks and, more particularly, to a method and apparatus for automated time domain monitoring in optical networks.

Generally, digital transmission systems deliver information, which is encoded as quantized signals, from a sender to a receiver. There are several parameters that characterize the quality of the transmission in these systems. One such parameter is the "bit error ratio" or BER. BER can be measured at any point in a transmission system, and may be used for fault detection and isolation.

There are many effects that contribute to degradation of a measured BER. For example, signal attenuation reduces signal amplitude, dispersion alters pulse shape, receiver and amplifier noise increase signal level ambiguity, and jitter creates uncertainty in the sampling point and affects other aspects of synchronization.

In an optical network, such as a Wavelength Division Multiplexing (WDM) network, data passes through many different types of network elements: wavelength converters and filters, wavelength add-drop multiplexer (ADM), cross-connects, and optical amplifiers. The network elements may perform multiple optical to electronic (O/E) and electronic to optical (E/O) conversions, or alternatively, may process the data in optical form. Although it is preferable to perform signal monitoring at network elements that include O/E and E/O converters, one can also tap and detect a signal at any point in a WDM network.

FIG. 1 illustrates a prior art optical signal monitoring system 100, which monitors optical signals on a fiber link by performing indirect SNR or average power level measurement. As shown, optical monitoring system 100 includes an optical fiber 110 carrying an input optical signal, optical power splitter 120, optical fiber 130 carrying output optical signal, wavelength selective filter 140, photodetector 150, electrical amplifier 160, and a spectrum analyzer 170. An incident optical signal present in optical fiber 110 is conveyed to output fiber 130 via coupler 120.

To monitor the input optical signal, an optical tap in coupler 120 extracts a small amount of signal power from optical fiber 110. Wavelength selective filter 140 selects a desired wavelength, and photodetector 150 converts the light associated with the selected wavelength into an electrical signal. The current from photodetector 150 is amplified by electrical amplifier 160, and subsequently measured by spectrum analyzer 170, or alternatively, an average value meter.

One of the signal characteristics measured by spectrum analyzer 170 is an estimated signal-to-noise ratio (SNR), which is commonly used to characterize a link performance

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in a WDM network. Optical domain spectral monitoring is typically used to estimate the SNR in optical networks. The signal is spectrally narrow, typically a few GHz. Assuming that the noise is slowly varying with wavelength, the optical noise level is measured at a wavelength slightly away from the channel's signal, where the ratio of this noise to the optical signal represents the optical SNR.

Presently, an optical spectrum analyzer or an equivalent (e.g., a Hewlett Packard wavemeter) is used to measure the characteristics of an input optical signal in a WDM network. Such instruments, however, have a number of disadvantages. First, these instruments are expensive and slow (i.e., require scanning across all wavelengths). Second, there are well-known inaccuracies that result from such optical measurements. Third, some sources of signal noise are not detectable with these instruments. For example, interferometric intensity noise is one such source of signal noise, which is not detectable in the optical domain. Fourth, any induced jitter or wander cannot be detected using these instruments. Finally, the required optical SNR for low BER depends not only on the signal rate but also on the details of the receiver design.

Optical networks, such as WDM networks, can provide flexible broadband connectivity. A unique feature of WDM network technology is rate and format transparency. For example, the bit rate  $f_{bit}$  of a signal may range from 25 Mb/s to 10 Gb/s. Furthermore, reconfigurable WDM networks perform highly variable route selection, a feature that is profoundly different from traditional point-to-point networks. At the periphery of such networks, any one set of users may employ at most a few line rates and formats. Within the network core, however, the full mix of rates and formats is encountered by most network elements. The route, line-rate, and format can be highly unpredictable and rapidly changing at any network element within a reconfigurable WDM network.

Like all other communication networks, it is desirable to monitor network transmission performance in WDM networks to anticipate problems before a user experiences poor service. Signal integrity and network link performance are closely monitored in traditional transmission systems, which operate at fixed line rates. These systems possess embedded signaling channels for diagnosis of transmission impairment and exchange of fault information.

For example, in Synchronous Optical Network (SONET) systems, the frame interval is continuously monitored along with verification of parity calculated on subsets of the bits within a frame. In these systems, loss of signal, loss of frame, and Bit Interleaved Parity 8 (BIP8) error rates are monitored and reported. Other transmission formats have their own embedded error detection.

Unlike traditional networks, however, WDM networks have less direct control over critical transmission parameters. Although many of the proposed WDM networks perform signal level management, they do not perform retiming, which is highly rate dependent and usually restrictive. When a WDM network performs little or no retiming, jitter management is delegated entirely to receivers at the user end. Accordingly, if the quality of the signal could be verified without full regeneration so that faults could be isolated to one subnetwork, it would facilitate implementation of multi-vendor interfaces for reconfigurable WDM networks.

Finally, interaction among protocol layers, such as locating faults when Internet Protocol (IP) routers or Asynchronous Transfer Mode (ATM) switches connect directly to

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optical networks, would be easier if a WDM network could dynamically determine the type of traffic it carries and test the quality of the traffic by checking for proper frame format and presence of errors. For example, when a network element in a WDM network detects an error in a signal, the network element could generate an alarm, facilitating the identification of the fault at the higher layer.

### DESCRIPTION OF THE INVENTION

It is desirable to have a method and apparatus for performing automated time domain monitoring in optical networks that overcome the above and other disadvantages of the prior art. Methods and apparatuses consistent with the present invention determine characteristics of an input optical signal by estimating a minimum time interval between transitions in the input signal, determining a clock signal based on the estimated minimum time interval, and performing a time domain measurement on the input signal based on the determined clock signal.

In one embodiment, an optical signal monitoring apparatus comprises a forward rate detector, clock recovery circuit, and a time domain measurement circuit. The forward rate detector estimates the minimum time interval between transitions in an input optical signal. Based on the estimated minimum time interval, the clock recovery circuit extracts a clock signal from the input signal. Using the extracted clock signal, the time domain measurement circuit samples the input signal, and determines in time domain the characteristics of the input signal.

Methods and apparatuses consistent with the invention have several advantages over the prior art. In an optical network, many different time domain measurements may be performed on an optical signal once a clock is extracted. The clock is essential for measuring an eye-pattern, from which one can determine activity on a particular wavelength, directly calculate signal power levels and noise, and calculate jitter. With automated measurement, both instantaneous fault and average non-fault behavior may be used in fault isolation. The clock may be used to identify bit boundaries and to read the signal. Pattern detection may be used to recognize, for example, SONET A1A2 framing or the special symbols used in block coding. This would allow network elements to perform many of the conventional bit-level performance monitoring operations, even without benefit of information from network management.

One may determine the type of traffic present on a wavelength (if it is in a local catalog) and inform network management of the traffic type and quality. This would obviously be useful for preventing provisioning errors (by detecting that the traffic type present does not match the traffic expected) when jumpers are connected incorrectly. Also, this could provide a means for billing the customer, even though the customer has a transparent connection and can send a wide range of rates and types of traffic. It could also provide a near-real-time inventory of traffic statistics to network management. None of these things can be done today in the optical domain, and using inflexible fixed regeneration sacrifices transparency—the regeneration circuit would need to be changed whenever the traffic type or speed is changed.

When signals cross administrative boundaries, for example between a local exchange carrier (LEC) and an inter exchange carrier (IEC) or between a private network and an LEC, it is necessary to determine that the signal is not impaired before it leaves one network and enters another. Today, this requires full regeneration and well-defined

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single-wavelength interfaces, such as SONET OC-3 or electrical DS-1 or DS-3. As bandwidth demands grow, it is desirable to eliminate this regeneration and permit transparent, multi-wavelength access by measuring the quality of the signal.

The description of the invention and the following description for carrying out the best mode of the invention should not restrict the scope of the claimed invention. Both provide examples and explanations to enable others to practice the invention. The accompanying drawings, which form part of the description for carrying out the best mode of the invention, show several embodiments of the invention, and together with the description, explain the principles of the invention.

### BRIEF DESCRIPTION OF THE DRAWINGS

In the Figures:

FIG. 1 illustrates a block diagram of a prior art optical signal monitoring system;

FIG. 2 illustrates a block diagram of a time domain optical signal monitoring apparatus, in accordance with an embodiment of the invention;

FIG. 3 illustrates a block diagram of a forward rate detector, in accordance with an embodiment of the invention;

FIG. 4 illustrates an emitter coupled logic (ECL) implementation of a minimum transition interval detection circuit, which uses pulse-width auto-correlations responsive to rising edge transitions, in accordance with an embodiment of the invention;

FIG. 5a illustrates a block diagram of a time domain measurement circuit, which performs self-calibrating waveform measurement suitable for network monitoring applications, in accordance with an embodiment of the invention;

FIGS. 5b, 5c, and 5d illustrate an eye-pattern for a signal at an input of a time domain measurement circuit, a synchronized calibration waveform, and a sampling pulse, respectively, in accordance with an embodiment of invention; and

FIG. 6 illustrates a block diagram of a time domain measurement circuit, in accordance with an embodiment of the invention.

### BEST MODE FOR CARRYING OUT THE INVENTION

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

FIG. 2 illustrates a block diagram of a time domain optical signal monitoring apparatus 200, in accordance with an embodiment of the invention. Signal monitoring apparatus 200 comprises a forward rate detection and selection circuit (forward rate detector or FWR) 210, programmable clock recovery circuit (PCR) 220, time domain measurement circuit 230, and a buffer amplifier 240.

An optical signal sample 152 is incident on photodetector 150, which produces a current received by a transimpedance amplifier 160. An optical signal sample 152 is obtained via an optical power splitter 120 from an optical fiber 110 carrying an input optical signal using a wavelength selective filter 140.

Output 164 of amplifier 160 connects to input 242 of buffer amplifier 240. Buffer amplifier 240 includes three equivalent analog outputs 244, 246 and 248. Output 244 connects to input 212 of forward rate detector 210. Output 246 connects to input 222 of clock recovery circuit 220. Output 248 connects to analog input 232 of time domain measurement circuit 230. The signal at input 242 of buffer amplifier 240 is an analog representation of optical signal sample 152.

Optical signal sample 152 can be characterized by a bit-rate  $f_{bit}$  when the optical signal sample 152 is a non-return-to-zero (NRZ) digital signal. Forward rate detector 210 produces a signal at output 214, which is an estimate of the bit-rate of the signal at input 242. In one embodiment, the signal at output 214 may be a digital representation of the estimated bit-rate.

Clock recovery circuit 220 includes a rate control input 224, which sets the particular frequency of operation in accordance with known techniques for clock recovery. Clock recovery circuit 220 generates a clock signal at output 226, which is synchronized with transitions in the signal at input 222 of clock recovery circuit 220 when rate control input 224 is set to a value that corresponds sufficiently close to  $f_{bit}$ . Rate control input 224 of clock recovery circuit receives a rate estimate signal from output 214 of forward rate detector 210.

As shown, clock recovery circuit 220 also includes a loss of lock signal output 228 that is active when clock output 226 is not synchronized to input 222. The signal at input 216 of forward rate detector 210 alters the algorithm used to determine the estimated bit rate of the signal applied to input 212. Different algorithms may be used depending on the current and past lock status of clock recovery circuit 220. In one embodiment, clock recovery circuit 220 may be implemented using known techniques for performing programmable clock recovery. Alternatively, clock recovery circuit 220 may be implemented in accordance with methods and apparatuses described in U.S. patent application Ser. No. 09/199,480, entitled "Method And Apparatus For Variable Bit Rate Clock Recovery."

Time domain measurement circuit 230 includes a clock input 234 and a rate input 236, which connect to output 226 of clock recovery circuit 220 and output 214 of forward rate detector 210, respectively. Using the clock signal at output 226 of clock recovery circuit 220, time domain measurement circuit 230 may perform waveform measurements on the analog signal at input 232. Time domain measurement circuit 230 may measure, for example, the eye-pattern in the optical signal sample 152, from which one can determine activity on a particular wavelength, directly calculate signal power levels and noise, and calculate jitter. Alternatively, time domain measurement circuit 230 may reconstruct the digital signal in optical signal sample 152 and subsequently assess particular characteristics of the digital signal.

Eye-pattern measurement is a time domain waveform measurement technique routinely employed to monitor and maintain digital transmission systems. The eye-pattern is an ensemble of average or superposition of pulse patterns corresponding to all different bit sequences. The ensemble may be obtained by sampling the signal waveform using a phase locked clock. The waveform can be characterized by the high and low mean signal levels  $\mu_{hi}$  and  $\mu_{lo}$ , and the variance in these levels  $\sigma_{hi}$  and  $\sigma_{lo}$ , respectively. The bit error rate (BER) of the signal can be accurately estimated from these eye-pattern parameters:

$$BER \approx \frac{1}{\sqrt{\pi}} \int_{Q_{opt}/\sqrt{2}}^{\infty} e^{-u^2} du = \frac{1}{2} \operatorname{erfc} \left[ \frac{Q_{opt}}{\sqrt{2}} \right]$$

where

$$Q_{opt} = \frac{\mu_{hi} - \mu_{lo}}{\sigma_{hi} + \sigma_{lo}}$$

In addition, jitter and wander can be assessed from the shape and variation of the transitions from low to high and vice versa. Eye-pattern measurements are an efficient diagnostic tool for assessing both slowly and rapidly changing transmission link performance. The eye-pattern provides a direct and consistent measure of signal parameters. An eye-pattern is especially important in WDM since the characteristics of the signal source and route may be highly variable.

The clock signal at output 226 of clock recover circuit 220 may be used to reconstruct the corresponding digital signal. Several measurements may be performed using the information contained in the recovered digital signal, depending on the transmission layer protocol. For example, byte alignment, framing, and error detection may be performed using a synchronized clock and knowledge of the bit rate. Pattern detection can be used to identify, for example, SONET A1A2 framing or the special symbols used in Gigabit Ethernet or Fiberchannel block coding. When the bit stream is associated with, for example, SONET, the error rate can be directly measured using the embedded Bit Interleaved Parity 8 (BIP8) bytes.

Furthermore, confirmation of bit synchronization may be used for rate reporting and as a criteria for usage billing. Additional monitoring functions could include determining source and destination address and cell or packet length and type. This information is useful for traffic monitoring and traffic characterization based on addressing and type as well as assessing network resource utilization.

FIG. 3 illustrates a block diagram of forward rate detector 210, in accordance with an embodiment of the invention. Alternatively, forward rate detector 210 may be implemented in accordance with methods and apparatuses described in U.S. patent application Ser. No. 09/199,480, entitled "Method And Apparatus For Variable Bit Rate Clock Recovery."

Forward rate detector 210 comprises a limiting amplifier 310, minimum transition interval detection circuit 320, transition counter 330, event rate counter 340, digital window comparator 350, successive approximation register 360, and a look-up table memory 370.

Forward rate detector 210 generates at output 204 a signal, which represents an estimate  $f_{est}$  for the value of the bit-rate  $f_{bit}$  of the signal applied at input 242. In one embodiment, the signal at output 204 has a binary weighted value that tracks the value of  $f_{bit}$ . In another embodiment, the signal at output 204 represents a set of one or more classifications of  $f_{bit}$ .

Minimum transition interval detection circuit 320 receives at input 322 an amplitude limited signal from amplifier 310 and at control signal input 324 a signal from register 360. The signal at control signal input 324 may, for example, include an m-bit wide digital word at lines 324<sub>1</sub>-324<sub>m</sub> (not shown), respectively. The signal at control input 324 programs n time reference intervals  $\tau_{r,1}$ - $\tau_{r,n}$ . The signal at output 326 may, for example, include an n-bit wide digital word at lines 326<sub>1</sub>-326<sub>n</sub> (not shown), respectively.

Minimum transition interval detection circuit 320 compares the time between consecutive transitions,  $\Delta t$ , of the signal at input 322 with each of the programmed time reference intervals  $\tau_{r-1}$  to  $\tau_{r-n}$ . Each of the  $n$  output lines 326<sub>1</sub>–326<sub>n</sub> corresponds to one of the  $n$  time interval comparisons. For each  $i=1, \dots, n$ , output 326<sub>i</sub> may be high if  $\Delta t < \tau_{r-i}$  and may be low if  $\Delta t > \tau_{r-i}$ . In particular, the probability that output 326<sub>i</sub> assumes a high value following consecutive transitions at input 322 is a monotonic function of the difference  $\Delta t - \tau_{r-i}$ .

Transition counter 330 generates a pulse at output 334 after a prescribed number,  $N_{i\_tran}$ , of consecutive transitions have occurred at input 332, where  $N_{i\_tran}$  is an integer with a value of, for example, 32.

Event rate counter 340 includes inputs 342, 344, and 346, which connect to output 314 of limiting amplifier 310, output 326 of minimum transition interval circuit 320, and output 334 of counter 330, respectively.

Event counter 340 generates a  $k$ -bit word at output 348, which includes lines 348<sub>1</sub>–348<sub>k</sub>, where the  $k$ -bit word depends on the number of times the output lines 326<sub>1</sub>–326<sub>n</sub> of transition detector 320 are high following a level transition in input signal 342 during the time interval between consecutive pulses at input 346.

Window comparator 350 includes an input 352, which connects to output 348 of event counter 340. Window comparator 305 also includes an output 354, which includes  $q$  signals in lines 354<sub>1</sub>–354<sub>q</sub> (not shown), respectively, where  $2 \leq q \leq n$ .

Register 360 includes inputs 362, 364, and 366, which connect to output 354 of window comparator 350, output 334 of counter 330, and loss of lock output 228, respectively. Register 360 also includes an output 368, which connects to input 324 of detector 320 and input 372 of look-up table memory 370. Output 374 of memory 370, which represents the signal at rate estimate output 204, connects to rate control input 224 of clock recovery circuit 220.

Forward rate detector 210 detects the bit-rate of optical signal sample 152 by estimating the minimum time interval between input signal transitions. Consecutive transitions of optical signal sample 152 can be assigned a time interval  $\Delta t$ . For a sufficiently large sample of transitions  $N_{i\_tran}$ , for example,  $N_{i\_tran}=32$ , the minimum value of the observed  $\Delta t$ , will be  $1/f_{bin}$  which may be represented as

$$\min_{i=1, N_{i\_tran}} \Delta t = 1/f_{bin}.$$

Minimum transition interval detection circuit 320 compares consecutive transition intervals against one or more reference time intervals. Event counter 340 and window comparator 350 classify the rate of responses from the interval comparisons present at output 326 of transition detector 320. The estimated bit rate is classified according to its relationship with the rates  $1/\tau_{r-i}$  corresponding to the reference time intervals  $\tau_{r-i}$ .

Forward rate detector 210 may estimate the bit-rate of optical signal sample 152 with  $m$ -bit resolution or may distinguish the bit-rate within a particular set of  $q+1$  rate categories. The two modes may be used simultaneously. For high resolution bit-rate tracking, one or more reference intervals  $\tau_{r-i}$  are adjusted by register 360 via output 368 as a result of the classification process performed by event counter 340 and window comparator 350 such that one or more reference intervals  $\tau_{r-i}$  match the minimum of  $\Delta t$ .

For rapid rate classification, one or more sets of reference time intervals are selected for which the corresponding rates

$1/\tau_{r-i}$  lie between the bit-rates of interest in optical signal sample 152. The classification process performed by event counter 340 and window comparator 350, in addition to interval assignment by register 360, determines which reference interval most likely includes the bit rate of optical signal sample 152. Register 360 may instruct detector 320 to use different sets of reference time intervals if clock recovery circuit 220 fails to achieve clock acquisition.

In one embodiment of the invention, precise rate measurements may be made with, for example,  $n=2$ ,  $m=10$ , and  $q=2$ .  $\tau_{r-1}=\tau_{r-2}$  may have a value that is monotonically related to the binary weighted value of the word represented by the collection of inputs lines 324<sub>1</sub>–324<sub>n</sub>. The monotonic relation may, for example, be linear or semi-logarithmic.

Event counter 340 assigns to output lines 348<sub>1</sub>–348<sub>k</sub> a binary weighted value corresponding to the total number of times output lines 326<sub>1</sub>–326<sub>n</sub> were individually high following a level transition at input 342 during the time interval between consecutive pulses applied to input 346 of event counter 340.

Window comparator 350 compares the binary weighted value at input 352 against a predetermined high value  $N_{hi}$  and a predetermined low value  $N_{lo}$ . Output line 354<sub>1</sub> is high if  $N_{hi}$  is smaller than the value at input 352, and output line 354<sub>2</sub> is high if  $N_{lo}$  is greater than the value at input 352.

Register 360 may be an  $m$  stage binary up-down counter whose count direction (hold, up or down) may be controlled by outputs 354<sub>1</sub> and 354<sub>2</sub>, which connect to inputs 362<sub>1</sub> and 362<sub>2</sub>, respectively. Depending on the number of pulses appearing at input 364 of register 360 during the time which input 366 may be at a high state, representing prolonged loss of lock by clock recovery circuit 220, the register may count by increments of, for example, 0 or  $\pm 1$  or by progressive steps of binary weight value of, for example, 0 or  $2^{n-step}$  with  $n$  step= $m, m-1, \dots, 0$ .

Look-up table 370 maps the  $m$ -bit word at output 368 into a bit-rate estimate signal 204 with a prescribed representation. Look-up table 370 may use, for example, a known transfer function relating the control input 324 and the response bit-rate  $f_{bin}$ , which may include a correction for known temperature dependencies, to convert the  $m$ -bit digital word at output 368 into the binary coded decimal word representing the estimated bit-rate.

In another embodiment, particular sets of rates may be rapidly distinguished by setting, for example,  $n=4$ ,  $q=n$ ,  $m=q+4$ , and  $k$  to a multiple of  $n$ . Accordingly, control input lines 324<sub>1</sub>–324<sub>3</sub> may select one of eight predetermined values for each of  $\tau_{r-1}$ ,  $\tau_{r-2}$ ,  $\tau_{r-3}$  and  $\tau_{r-4}$ .

Each set of  $k/n$  output lines 348<sub>1</sub>–348<sub>k</sub> includes a binary weighted value equal to the total number of times the corresponding input 326<sub>i</sub>, for  $i=1, \dots, n$ , is high following transitions in the signal at input 342 during the time interval between consecutive pulses at input 346.

Each of output lines 354<sub>1</sub>–354<sub>q</sub> corresponds to a  $k/n$  subset of inputs such that an output line 354<sub>i</sub> is high if the word represented by the corresponding  $k/n$  bits includes a binary weighted value that exceeds a predetermined value  $N_{hi}$ .

Register 360 may include a  $q$  input priority encoded with  $q+1$  outputs,  $q+1$  latches enabled by pulses applied to input 360, and an  $m-q-1=3$  bit binary counter.

Look-up table 370 may assign the appropriate rate to the  $m$ -bit digital word at output 368, which connects to input 324 of minimum transition interval detection circuit 320 and input 372 of look-up table 370. Look-up table 370 may, for example, include an  $m \times r$  memory. The memory output locations may include  $r$ -bit representations of the rates

corresponding to references time intervals selected by the control signal at control input 324.

FIG. 4 illustrates an emitter coupled logic (ECL) implementation of minimum transition interval detection circuit 320, which uses pulse-width auto-correlations responsive to rising edge transitions, in accordance with an embodiment of the invention. Minimum transition interval detection circuit 320 comprises an input 322, control input 324, output 326, ECL gate 410 D-type latching comparator 430, and a programmable delay element 408. Programmable delay element 408 includes an ECL OR/NOR gate 420, capacitor 440, voltage reference 450, transistor 460, and programmable current sources 444 and 464.

Input 322 connects to inputs 412 and 422 of gate 410 and OR/NOR gate 420, respectively. Non-inverting output 416 of gate 410 connects to second input 424 of OR/NOR gate 420. Inverting output 418 of gate 410 drives clock input 436 of latching comparator 430. Gate 420 includes a non-inverting output 426 and an inverting output 428. Output 428 is an open-emitter, allowing gate 420 to perform a current gating function. Capacitor 440 connects to output 426 and node 442.

Node 442 connects to open-emitter output 428 and controlled current source 444. Capacitor 440 is charged by current from output 428 and is discharged at a controlled rate by the current  $I_{444}$  from source 444. Non-inverting data input 432 of latched comparator 430 senses the voltage at node 442.

Reference voltage 450 connects to the base of transistor 460 whose emitter is connected to node 462. Controlled current source 464 also connects to node 462. Current sources 444 and 464 include control inputs 446 and 466, respectively, which are both connected to control input 324. Inverting data input 434 of latched comparator 430 senses the voltage on node 462.

Comparator 430 senses the voltage difference between inputs 432 and 434 when clock input 436 is low. Output 438 of latching comparator 430 is updated on the rising edge transition of enable input 436. Latching comparator 430 may, for example, be a D-type flip flop with differential data inputs. Detector output 326 connects to output 438 of latching comparator 430.

In the embodiment of FIG. 4, minimum transition interval detection circuit 320 responds to a rising edge transition of the digital signal applied to input 322 and determines whether the subsequent falling edge transition occurs before or after a programmable reference time interval  $\tau_r$  has elapsed. In an alternative embodiment, multiple minimum transition interval detection circuit 320 connected in parallel may each receive a replica of the signal at input 322 with opposing polarity, and may subsequently measure the minimum transition interval associated with both rising and falling edge transitions.

The quiescent state of minimum transition interval detection circuit 320 is defined when input 322 is low. In the quiescent state, gate output 418 is high and output 416 is low. When input 322 and output 416 are low, gate output 426 is low and output 428 is high. Output 428 conducts most of the current from source 444. The voltage across capacitor  $C_{440}$  in the quiescent state is the difference between  $V_{428}^{hi}$  at output 428, for example  $-0.8V$ , and  $V_{426}^{low}$  at output 426, for example  $-1.8V$ .

A reference voltage  $V_{462}$  is created at node 462 by voltage reference 450, transistor 460, and current source 464. The reference voltage may be chosen to be lower than the quiescent voltage at output 428, for example  $-1.5V$ . The quiescent voltage at output 428 may be altered by changes

in current  $I_{444}$  flowing into current source 444. Current sources 444 and 464 have related outputs through their common control via inputs 324. The change in the quiescent voltage at output 428, which is associated with the current through source 444, may be matched by the change in voltage at node 462 associated with current source 464. Comparator 430 is not responsive to the like current dependent offsets applied simultaneously to differential inputs 432 and 434.

Gate 420 and gate 410 respond when input signal 322 transitions from low to high after a gate propagation delay, output 416 and output 426 transition from low to high, output 418 transitions from high to low, and output 428 ceases to conduct current from source 444. The positive transition at output 426 to  $V_{426}^{hi}$  drives node 442 high, while the current from source 444 causes the voltage at node 442 subsequently decrease with time. The voltage at node 442 will equal the voltage at node 462 after period  $\tau_r$  has elapsed, and may be represented as follows:

$$I_{444}\tau_r = C_{440}(V_{428}^{hi} + V_{426}^{hi} - V_{426}^{low} - V_{462}) - Q_{428},$$

where  $Q_{428}$  is the charge absorbed by output 428 as it goes inactive.

Gate 410 responds to a subsequent high-to-low transition of input 322 and after a gate propagation delay, output 416 transitions high to low, and output 418 transitions low to high. The low-to-high transition at output 418 activates comparator clock input 436. If clock input 436 transitions from high to low before  $\tau_r$  has elapsed, output 438 will be high. Otherwise, output 438 will be low. A high level at output 438 indicates  $1/f_{bit} < \tau_r$ .

Gate 420 responds to the high-to-low transition of output 416, two gate delays following the high-to-low transition of input 322, with output 428 becoming active and raising the voltage at node 442 to  $V_{428}^{hi}$  while output 426 goes low. The connection of output 416 to input 424 delays the response of gate 420 to falling edge input transitions so as not to disturb the voltage at node 442 while comparator 430 is being latched.

FIG. 5a illustrates a block diagram of time domain measurement circuit 230, which performs self-calibrating waveform measurement suitable for network monitoring applications, in accordance with an embodiment of the invention. Measurement circuit 230 includes an analog input 232, recovered clock input 234, sampling rate clock 502, clock divide-by-2 circuit 510, limiting amplifier 516, D-type flip-flop 520, counter 530, programmable delay generator 540, sampler driver 550, sampling circuits 560 and 570, two channel analog multiplexer 580, analog-to-digital (A/D) converter 586, and an event accumulator 590. Clock divide-by-2 circuit 510, limiting amplifier 516, D-type flip-flop 520, sampling circuit 570, and input 234 constitute a time base auto-calibration circuit.

The analog signal at input 232, which connects to output 248 of buffer amplifier 240, is a replica of optical signal sample 152. Sampler 560 includes input 562, which connects to input 232. Since input 234 connects to clock recovery circuit 220, the clock signal at input 234 is synchronous with transitions in the signal at input 232.

Clock divide-by-2 circuit 510 includes an output 514, which connects to input 522 of D-type flip-flop 520 and input 518 of limiting amplifier 516. The signal at output 514 is a square wave pulse train with transitions at  $1/f_{bit}$  intervals synchronized with the signal at input 234. The signal at output 514 may be used, for example, to perform time base calibration.

Limiting amplifier 516 includes an output 519, which connects to an input 572 of sampler 570. The amplitude of the signal at output 519 may include a predetermined value, making the signal useful for amplitude calibration purposes.

D-type flip-flop 520 includes an input 524, which connects to a sampling rate clock 502, and an output 526, which connects to input 532 of counter 530 and input 542 of programmable delay generator 540. The rate of the waveform sampling process may be controlled by clock 502.

Counter 530 includes a digital output 534, which connects to delay control input 544 and write address input 594 of event accumulator 590. Pulse output 548 connects to trigger input 552 of sampler driver 550. Sampler driver 550 produces a very short pulse at output 554 in response to a falling edge transition applied to input 552.

Programmable delay generator 540 includes a trigger input 542, delay control input 544, rate range input 546, and a pulse output 548. Programmable delay 540 generates a delayed falling edge pulse at output 548 in response to a rising edge transition at input 542. The falling edge at output 548 is delayed by a period of time  $\tau_{OS}$ , which is determined by delay control input 544 and rate range input 546. The delay period  $\tau_{OS}$  is coarsely tuned by input 546 and finely tuned by input 544. Rate range input 546 receives a rate estimate signal at input 236.

Sampler 560 includes a gating input 564 and output 566. Sampler 570 includes a gating input 574 and output 576. Gating inputs 564 and 574 both connect to sampler driver output 554. A short pulse applied to gating inputs 564 and 574 cause samplers to transiently measure the voltage appearing at their respective inputs 562 and 572.

Samplers 560 and 570 include signal outputs 566 and 576, respectively, which are connected to inputs 581 and 582, respectively, of analog multiplexer 580. Analog multiplexer 580 holds the voltage level applied to inputs 581 and 582, and alternately presents these voltages to A/D converter 586. Digital output 588 from A/D converter 586 is received by write input 592.

Event accumulator 590 includes a write input 592, write address 594, read output 596, and a read address input 598. Event accumulator 590 receives at input 592 m-bit digital words from A/D converter 586 corresponding to voltage levels on inputs 581 and 582. Event accumulator 590 receives at input 594 p-bit digital words corresponding to the delay applied to the trigger pulse, which initiated acquisition of the waveform samples appearing as voltage levels at inputs 581 and 582.

Event accumulator 590 performs an auto-regressive average of the number of times a particular word appears at input 592 coincident with another particular word at input 594. Event accumulator 590 may, for example, comprise an  $m \times p \times q$  random access memory and an arithmetic logic unit. It will be recognized that the contents of the registers in accumulator 590 constitute a histogram of voltage levels as a function of delay time for both the analog signal at input 232 and the square wave signal at output 519. The set of histograms for the analog signal at input 232 constitute an eye-diagram for the measured waveform. The set of histograms for the square wave signal at output 519 constitute a measured calibration waveform. The two histogram arrays, one for the eye-pattern and one for the calibration waveform, may be accessed at output 596 via addressing by read address input 598.

FIG. 5b illustrates an eye-pattern for the analog signal at input 232 of time domain measurement circuit 230. FIG. 5c illustrates the square wave calibration signal at output 519 of limiting amplifier 516. A rising edge transition associated

with the triggering of sampler driver 550 is shown. FIG. 5d illustrate the sampling pulse at output 554 of sampler driver 550. As shown, the sampling pulse at output 554 is delayed by time  $\tau_{OS}$ .

The sampling pulse at output 554 is finely stepped across the measured waveform. The period of the measured waveform may vary from 100 psec to 100 nsec, requiring different size steps for  $\tau_{OS}$ . The step size of  $\tau_{OS}$  is represented by a controlled rate signal at input 546 to programmable delay generator 540. The estimated rate signal at input 236 provides the necessary information to automatically chose the appropriate set size for  $\tau_{OS}$ .

Eye-pattern measurements require accurate correlation of amplitude and time. To produce a delay  $\tau_{OS}$  that has low jitter and a precisely controlled value, more complex circuits known in the art may be used to achieve both accuracy and low jitter. Complex circuits, however, may not be appropriate for performing automated waveform measurement in WDM networks.

Accordingly, programmable delay generator 540 may comprise, for example, delay element 408 shown in FIG. 4, which is simple, has low jitter, and has a monotonic response to the control currents. Measurement of calibration signal 519 performed simultaneously with measurement of the analog signal at input 232 provides an internal time reference for calibrating the delay  $\tau_{OS}$ . In one embodiment, the time values associated with the waveform voltage samples may be calculated by interpolating the time values assigned to measured transitions in calibration waveform 519.

FIG. 6 illustrates a block diagram of time domain measurement circuit 230, in accordance with an embodiment of the invention. Measurement circuit 230 comprises a decision flip-flop 620, shift register 630, rate-addressed look-up table 640, and byte-processing circuit 650.

Decision flip-flop 620 includes an analog input 622, clock input 624, and a digital output 626. Shift register 630 includes a serial input 632, clock input 634, and a parallel data output 636. Look-up table 640 includes a rate estimate input 642 and a data field descriptor output 644. Byte-processing circuit 650 includes a parallel data input 652, data field descriptor input 654, and a clock input 656.

Optical signal sample 152 may be an optical sampling means as shown in FIG. 1. Alternatively, optical signal sample 152 may be obtained from an optical fiber used for accessing an optical network. As shown in FIG. 6, light from optical signal sample 152 is incident on photodetector 150 whose current output is received by input 162 of electrical amplifier 160. Output 164 of amplifier 160 connects to input 242 of buffer amplifier 240, which generates three replicas of input signal 242 at outputs 244, 246, and 248.

Output 244 connects to input 212 of forward rate detector 210. Output 246 connects to input 222 of clock recovery 220. Output 248 connects to analog input 622 of decision flip-flop 620. Rate control input 224 of clock recovery circuit 220 connects to rate estimate output 214 of forward rate detector 210. Forward rate detector 210 rapidly estimates the bit-rate of input signal 152. The rate estimate signal at input 214 sets rate control input 224 of clock recovery circuit 220 so that clock recovery circuit 220 can appropriately respond to the bit-rate of input signal 152.

When forward rate detector 210 is implemented as a discrete rate detector, the step of rate estimation may be accomplished within, for example, 8 to 32 signal transitions following the onset of input signal 152. Rate detector 210 accepts control input 216 from loss of lock output 228 of clock recovery circuit 220. Recovered clock output 226 connects to clock inputs 624 and 634 of decision circuit 620



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and shift register 630, respectively. Output 226 also connects to clock input 656.

Decision flip-flop 620 converts the analog signal at input 622 into a re-timed digital bit-stream at output 626. Shift register 630 converts the serial bit stream into a set of time shifted bit streams.

Look-up table 640 receives at input 642 the estimated rate output 214. Different rate specific information may be stored in look-up table 640, including, for example, byte alignment bit patterns, frame alignment bit-patterns, location of address data, location of error detection data, location of error correction data, and location cell or packet description data. The desired rate specific bit patterns and locations may be provided at output 644.

There are several additional time domain measurements, which may be performed with the recovered clock at output 226 in addition to error detection as previously mentioned. For example, the clock may be used to recover the bit stream so that appropriate computations, such as BIP8, may be performed. Confirmation of bit synchronization may be used for rate reporting and as criteria for usage billing. Other bit level functions may include traffic monitoring and traffic characterization based on addressing and type as well as assessing network resource utilization.

While it has been illustrated and described what are at present considered to be preferred embodiments and methods of the present invention, it will be understood by those skilled in the art that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the invention.

In addition, many modifications may be made to adapt a particular element, technique or implementation to the teachings of the present invention without departing from the central scope of the invention. Therefore, it is intended that this invention not be limited to the particular embodiments and methods disclosed herein, but that the invention include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A method for determining time domain characteristics of a monitored input signal from an optical network comprising the steps of:

estimating a minimum time interval between consecutive transitions in the input signal;  
determining a variable bit rate of the input signal based on the estimated minimum time interval;  
recovering the input signal's clock signal based on the determined bit rate; and  
performing a time domain measurement on the input signal based on the determined bit rate and the recovered clock signal.

2. A method for determining time domain characteristics of a monitored input signal from an optical network comprising the steps of:

estimating a minimum time interval between transitions in the input signal;  
determining a variable bit rate of the input signal based on the estimated minimum time interval;  
recovering the input signal's clock signal based on the determined bit rate; and  
performing a time domain measurement on the input signal based on the recovered clock signal, said performing step including the step of reconstructing a digital signal from the monitored input signal by sampling the input signal based on the recovered clock signal.

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3. The method of claim 2, wherein the reconstructing step includes the step of:

sampling one or more bit intervals in the input signal.

4. The method of claim 2, wherein the reconstructing step includes the step of:

sampling the input signal at a midpoint of a bit interval in the input signal.

5. The method of claim 1, wherein the performing step includes the steps of:

determining a rate specific signal characteristic of the input signal based on the determined bit rate; and  
measuring the input signal based on the rate specific signal characteristic.

6. The method of claim 5, wherein the step of determining the rate specific signal characteristic includes the step of:

determining a byte alignment bit pattern associated with the input signal based on the determined bit rate.

7. The method of claim 5, wherein the step of determining the rate specific signal characteristic includes the step of:

determining a frame alignment bit pattern associated with the input signal based on the determined bit rate.

8. The method of claim 5, wherein the step of determining the rate specific signal characteristic includes the step of:

determining location of address data associated with the input signal based on the determined bit rate.

9. The method of claim 5, wherein the step of determining the rate specific signal characteristic includes the step of:

determining location of error detection data associated with the signal input based on the determined bit rate.

10. The method of claim 5, wherein the step of determining the rate specific signal characteristic includes the step of:

determining location of error correction data associated with the input signal based on the determined bit rate.

11. The method of claim 5, wherein the step of determining the rate specific signal characteristic includes the step of:

determining location of packet descriptive data associated with the input signal based on the determined bit rate.

12. The method of claim 5, wherein the step of determining the rate specific signal characteristic includes the step of:

determining location of cell description data with the input signal based on the determined bit rate.

13. The method of claim 1, wherein the performing step includes the step of:

identifying a protocol associated with the input signal based on the determined bit rate.

14. The method of claim 1, wherein the performing step includes the step of:

determining a location of information associated with the input signal based on the determined bit rate.

15. The method of claim 14, wherein the step of determining the location includes the step of:

extracting the information at the determined location in the input signal.

16. A method for determining time domain characteristics of a monitored input signal from an optical network comprising the steps of:

estimating a minimum time interval between transitions in the input signal;  
determining a variable bit rate of the input signal based on the estimated minimum time interval;  
recovering the input signal's clock signal based on the determined bit rate; and  
performing a time domain measurement on the input signal based on the recovered clock signal, the performing step including the steps of:

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sampling the recovered clock signal and the input signal at a plurality of times to generate a clock signal histogram and an input signal histogram; and using the clock signal histogram to calibrate the timing sequence of the sampled input signal histogram.

17. A method for determining time domain characteristics of a monitored input signal from an optical network comprising the steps of:

estimating a minimum time interval between transitions in the input signal;

determining a variable bit rate of the input signal based on the estimated minimum time interval;

recovering the input signal's clock signal based on the determined bit rate; and

performing a time domain measurement on the input signal based on the recovered clock signal, the performing step including the steps of:

sampling the recovered clock signal and the input signal at a plurality of times to generate a clock signal histogram and an input signal histogram; and using the clock signal histogram to calibrate the amplitude of the sampled input signal histogram.

18. The method of claim 1, wherein the estimating step includes the step of:

determining a variable bit rate of the input signal based on the estimated minimum time interval.

19. A method for determining time domain characteristics of a monitored input signal from an optical network comprising the steps of:

estimating a minimum time interval between transitions in the input signal;

determining a variable bit rate of the input signal based on the estimated time interval;

recovering the input signal's clock signal based on the determined bit rate; and

performing a time domain measurement on the input signal based on the recovered clock signal, and wherein the estimating step includes the steps of:

generating a plurality of test pulses that correlate to the transitions in the input signal; and

adjusting the duration of each of the plurality of test pulses such that the minimum time intervals between the transitions in the input signal match the durations of the corresponding plurality of pulses.

20. A method for determining characteristics of an input signal comprising the steps of:

estimating a minimum time interval between transitions in the input signal;

determining a clock signal based on the estimated minimum time interval; and

performing a time domain measurement on the input signal based on the determined clock signal;

wherein the estimating step includes the steps of:

generating a set of delayed input signals using a set of programmable delay times, respectively;

comparing the transitions in the input signal with the set of delayed input signals; and

identifying the nearest predetermined delay times that are before and after the minimum transition time interval between the transitions in the input signal.

21. The method of claim 20, wherein the generating step includes the step of:

resetting one or more of the programmable delay elements after the comparing step.

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22. A method for determining characteristics of an input signal comprising the steps of:

estimating a minimum time interval between transitions in the input signal;

determining a clock signal based on the estimated minimum time interval; and

performing a time domain measurement on the input signal based on the determined clock signal;

wherein the estimating step includes the steps of:

generating a set of delayed input signals using a set of programmable delay elements delaying the input signal based on a set of predetermined delay times, respectively;

comparing the transitions in the input signal with the set of delayed input signals; and

adjusting one or more of the programmable delay elements, such that minimum time intervals between the transitions in the input signal match one or more of the set of predetermined delay times.

23. The method of claim 22, wherein the generating step includes the step of:

resetting one or more of the programmable delay elements after the comparing step.

24. An apparatus for determining time domain characteristics of a monitored input signal from an optical network comprising:

a forward rate detector that determines the input signal's bit rate by measuring the minimum time interval between consecutive transitions in the input signal, said forward rate detector including a transition detector and line rate estimation circuitry;

a clock recovery circuit that recovers the input signal's clock signal based on the determined bit rate; and

a measurement circuit that performs a time domain measurement on the input signal based on the recovered clock signal.

25. An apparatus for determining the time domain characteristics of a monitored input signal from an optical network comprising:

a forward rate detector that determines the input signal's bit rate by estimating a minimum time interval between transitions in the input signal;

a clock recovery circuit that recovers the input signal's clock signal based on the determined bit rate; and

a measurement circuit that performs a time domain measurement on the input signal based on the recovered clock signal, the measuring circuit comprising:

a delay generator that generates a first pulse synchronized to the recovered clock signal;

a sampler driver that generates a second pulse in response to the first pulse; and

a first sampler that measures a plurality of instantaneous values of the input signal gated by the second pulse in order to generate a histogram of the input signal.

26. An apparatus for determining time domain characteristics of a monitored input signal from an optical network comprising:

a forward rate detector that determines the input signal's bit rate by estimating a minimum time interval between transitions in the input signal;

a clock recovery circuit that recovers the input signal's clock signal based on the determined bit rate; and

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a measurement circuit that performs a time domain measurement on the input signal based on the recovered clock signal, the measurement circuit comprising:  
a decision circuit that reconstructs a digital signal from the monitored input signal by sampling the input signal based on the recovered clock signal.

27. The apparatus of claim 26, wherein the measurement circuit further comprises:

a converter that generates a stream based on the sampled input signal;  
a storage device storing a set of rate specific signal characteristics that are referenced based on the determined bit rate; and  
a processing circuit that measures the stream based on the set of rate specific signal characteristics.

28. The apparatus of claim 27, wherein the set of signal characteristics include a byte alignment bit pattern.

29. The apparatus of claim 27, wherein the set of signal characteristics include a frame alignment bit pattern.

30. The apparatus of claim 27, wherein the set of signal characteristics include location of address data.

31. The apparatus of claim 27, wherein the set of signal characteristics include location of error detection data.

32. The apparatus of claim 27, wherein the set of signal characteristics include location of error correction data.

33. The apparatus of claim 27, wherein the set of signal characteristics include packet description data.

34. The apparatus of claim 27, wherein the set of signal characteristics include cell description data.

35. An apparatus for determining the time domain characteristics of a monitored input signal from an optical network comprising:

a forward rate detector that determines the input signal's bit rate by estimating a minimum time interval between transitions in the input signal;  
a clock recovery circuit that recovers the input signal's clock signal based on the determined bit rate; and  
a measurement circuit that performs a time domain measurement on the input signal based on the recovered clock signal, the measurement circuit comprising a storage device storing a location of data associated with the input signal wherein the storage device is referenced based on the determined bit rate.

36. The apparatus of claim 35, wherein the measurement circuit further comprises:

a processing circuit that extracts information from the input signal based on the location data.

37. An apparatus for determining time domain characteristics of a monitored input signal from an optical network comprising:

a forward rate detector that determines the input signal's clock signal based on the determined bit rate; and  
a measurement circuit that performs a time domain measurement on the input signal based on the recovered clock signal, the measurement circuit comprising:  
a delay generator that generates a first pulse synchronized to the recovered clock signal;  
a sampler drive that generates a second pulse in response to the first pulse;  
a first sampler that measures a plurality of instantaneous values of the input signal gated by the second pulse to generate an input signal histogram; and  
a second sampler that measures a plurality of instantaneous values of the recovered clock signal gated by the second pulse to generate a clock signal histogram used to calibrate the input signal histogram.

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38. An apparatus comprising:

a forward rate detector that estimates a minimum time interval between transitions in an input signal;  
a clock recovery circuit that determines a clock signal based on the estimated minimum time intervals; and  
a measurement circuit that performs a time domain measurement on the input signal based on the determined clock signal;

wherein the forward rate detector comprises a minimum transition interval detection circuit that compares time intervals between consecutive transitions in the input signal with one or more reference intervals, the minimum transition interval detection circuit comprising:  
a delay element that delays a first transition in the input signal by a first predetermined delay time and delays a second transition in the input signal by a second predetermined delay time; and  
a comparator that compares the delayed first transition with the second transition.

39. An apparatus comprising:

a forward rate detector that estimates a minimum time interval between transitions in an input signal;  
a clock recovery circuit that determines a clock signal based on the estimated minimum time interval; and  
a measurement circuit that performs a time domain measurement on the input signal based on the determined clock signal;

wherein the forward rate detector comprises

a minimum transition interval detection circuit that compares time intervals between consecutive transitions in the input signal with one or more reference intervals, the minimum transition interval detection circuit comprising  
a set of delay elements that generate a set of delayed input signals based on a set of predetermined delay times; and  
a comparator that compares transitions in the set of delayed input signals with the transitions in the input signal.

40. The apparatus of claim 39, wherein the forward rate detector comprises:

an encoder that identifies nearest ones of the set of predetermined delay times that are before and after the minimum time interval between the transitions in the input signal.

41. An apparatus comprising:

a forward rate detector that estimates a minimum time interval between transitions in an input signal;  
a clock recovery circuit that determines a clock signal based on the estimated minimum time interval; and  
a measurement circuit that performs a time domain measurement on the input signal based on the determined clock signal;

wherein the forward rate detector comprises:

a minimum transition interval detection circuit that compares time intervals between consecutive transitions in the input signal with one or more programmable reference intervals; and  
a register that adjusts the programmable reference intervals such that one or more of the adjusted reference intervals match the minimum time interval between the transitions in the input signal.

\* \* \* \* \*



US006265999B1

(12) **United States Patent**  
**Prucnal**

(10) **Patent No.:** **US 6,265,999 B1**  
(45) **Date of Patent:** **Jul. 24, 2001**

(54) **HIGH-SPEED SERIAL-TO-PARALLEL AND ANALOG-TO-DIGITAL CONVERSION**

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(\*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(21) **Appl. No.:** **08/941,364**

(22) **Filed:** **Sep. 30, 1997**

(51) **Int. Cl.<sup>7</sup>** ..... **H03N 1/00**

(52) **U.S. Cl.** ..... **341/137; 341/155; 359/237**

(58) **Field of Search** ..... **341/155, 100, 341/137, 139; 359/237, 245, 340, 341**

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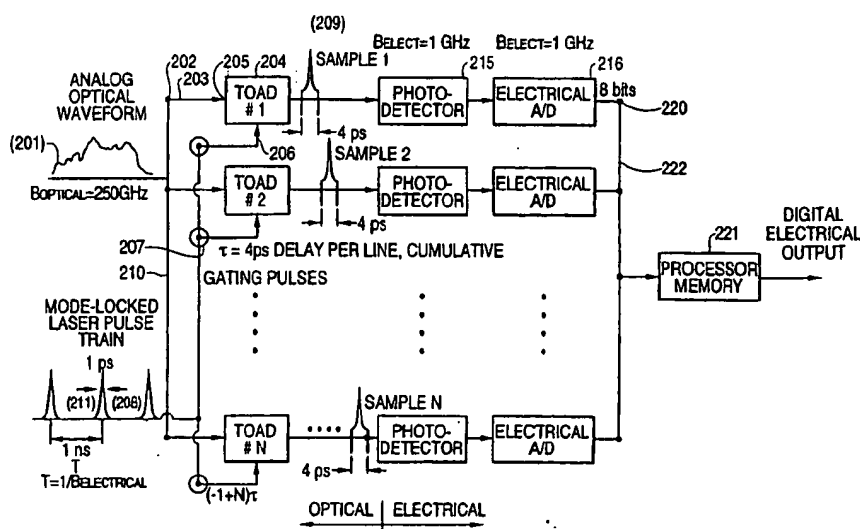
*Primary Examiner*—Peguy JeanPierre

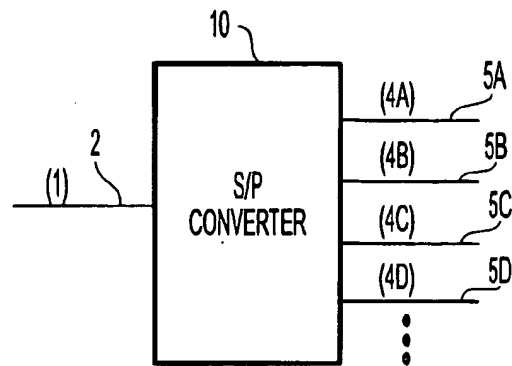
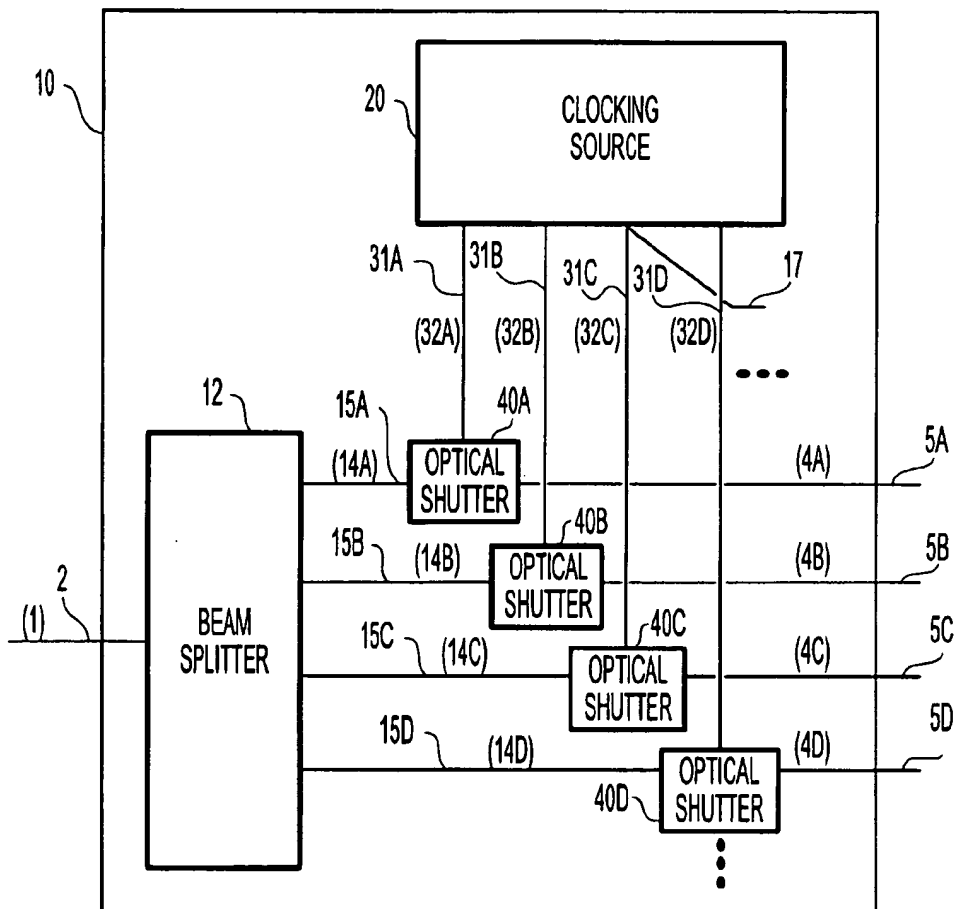
(74) *Attorney, Agent, or Firm*—Pennie & Edmonds LLP

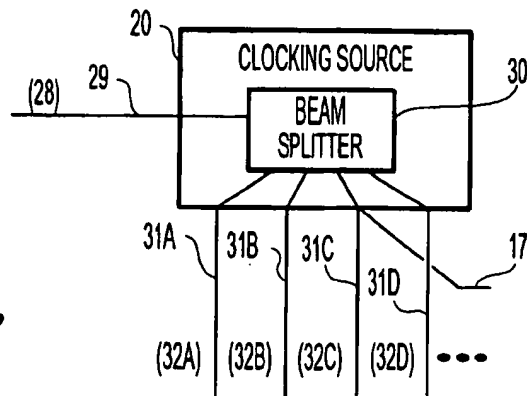
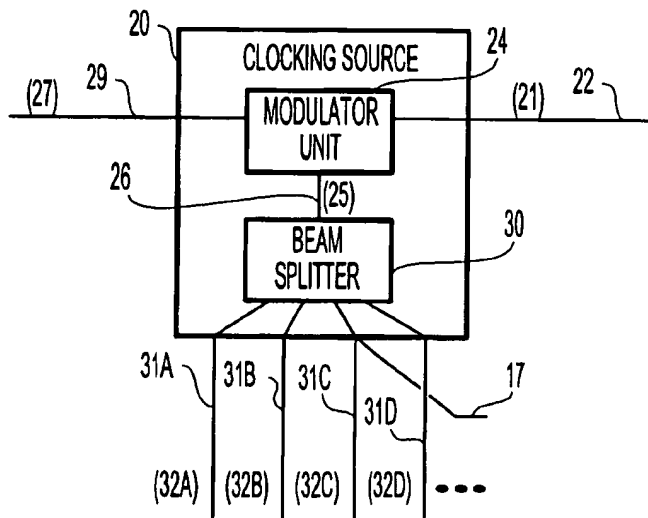
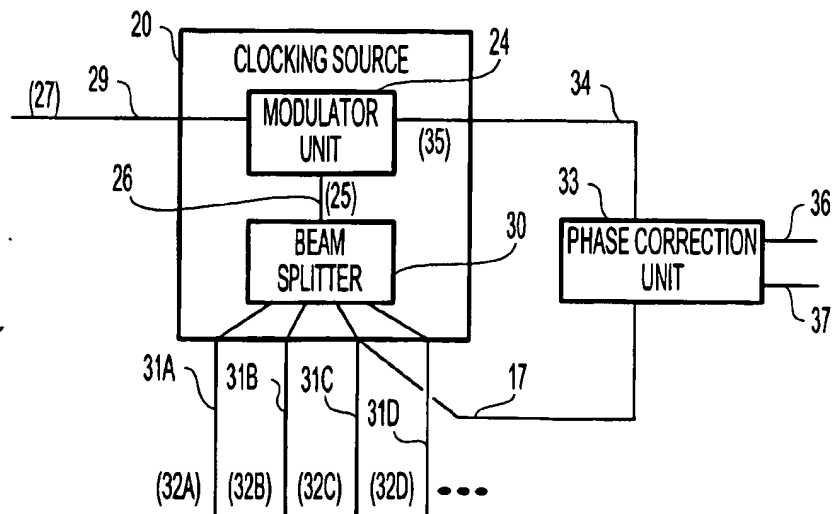
(57) **ABSTRACT**

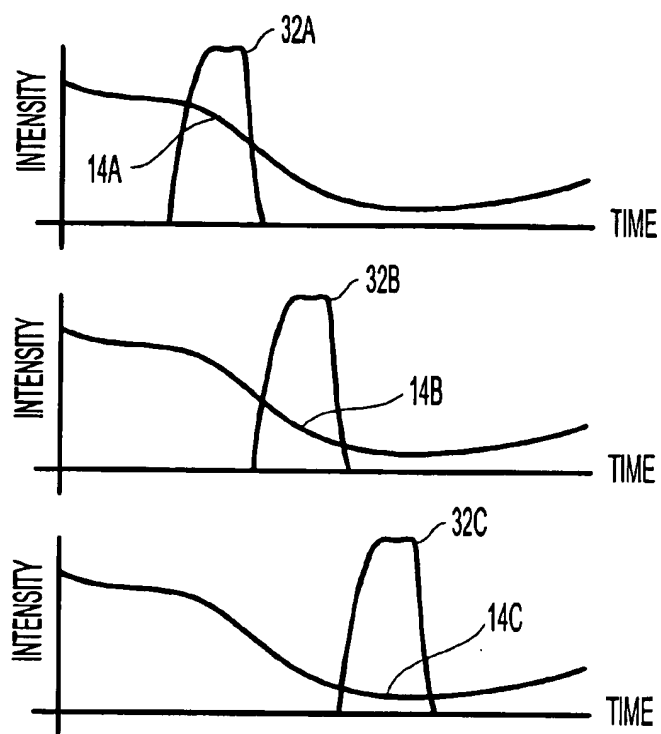
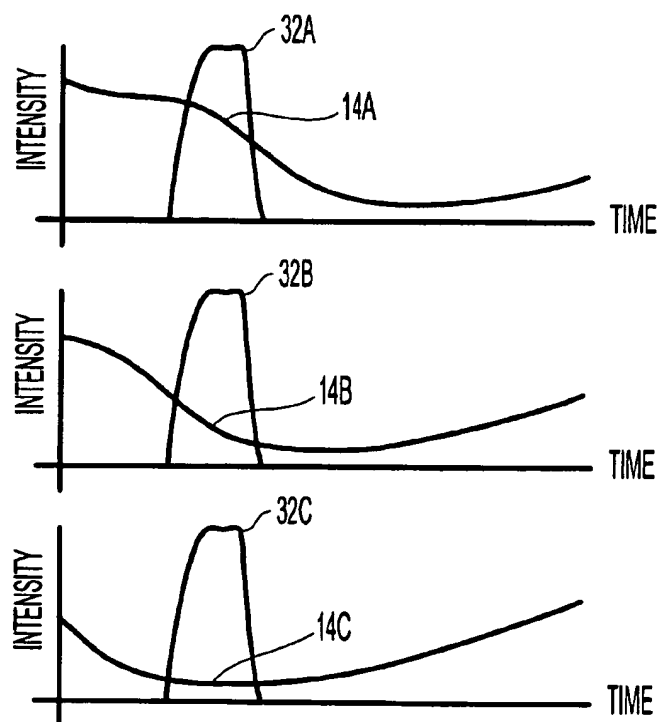
An optical-to-electrical converter includes an input port configured to receive an optical signal. The converter further includes a splitter configured to split the received optical signal into a plurality of optical signals. An optical stage has a plurality of parallel stages, and each parallel stage receives a corresponding one of the plurality of identical signals and outputs a corresponding one of a plurality of sampled optical signals within a corresponding sampling window. A plurality of delay circuits receive a clock signal having a plurality of clock pulses separated by a clock period. The delay circuits respectively output a plurality of control pulses at a plurality of delayed timings with respect to each clock pulse of the clock signal. An electrical stage receives the plurality of sampled optical signals and processes the optical signals at a sampling rate corresponding to the clock period of the clock signal.

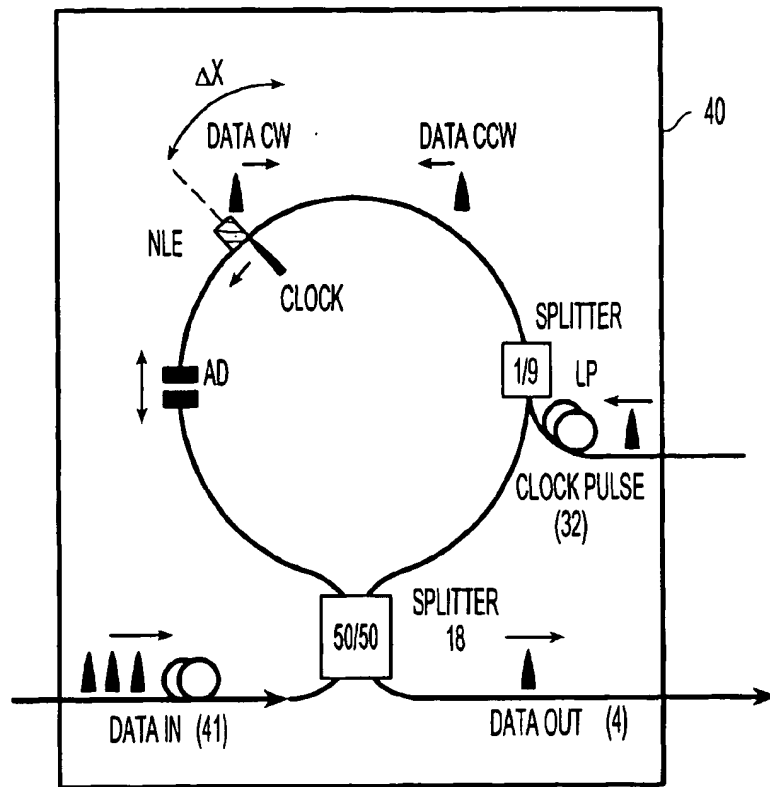
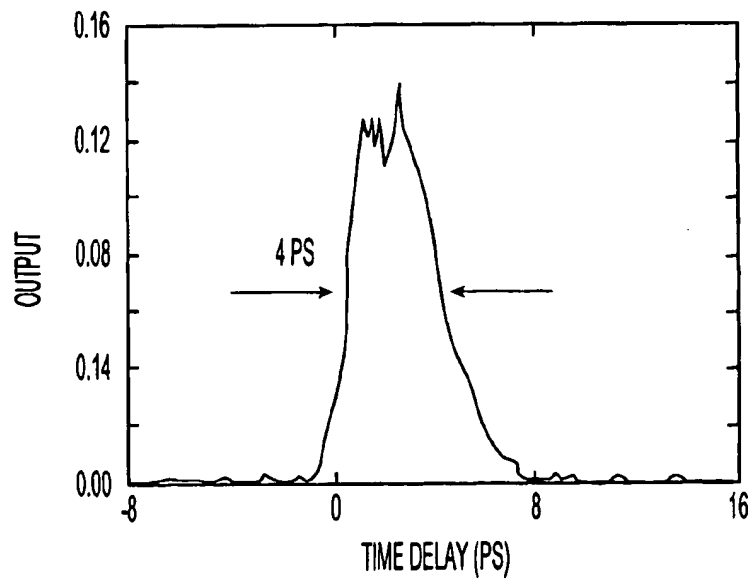
**34 Claims, 10 Drawing Sheets**



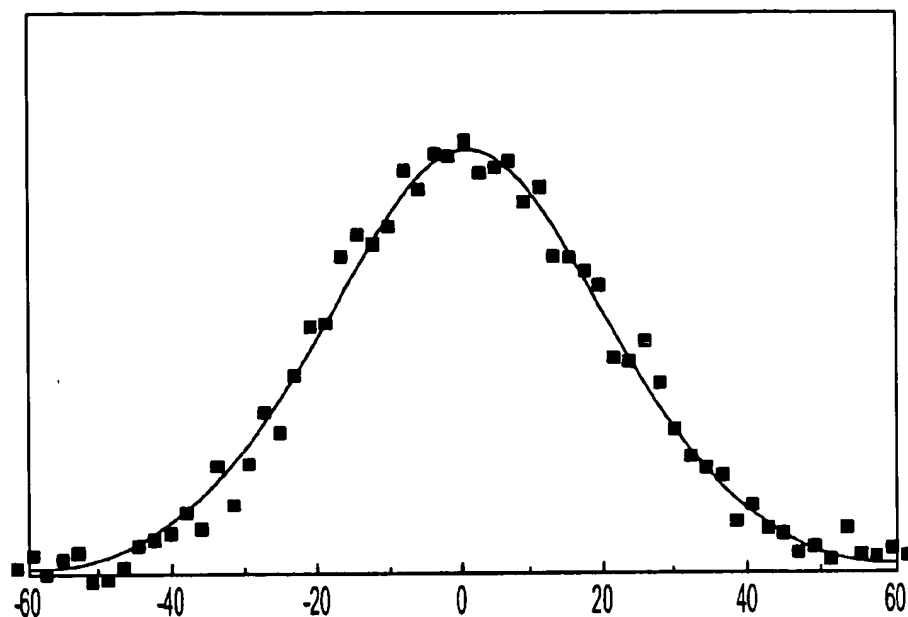
*Fig. 1**Fig. 2*

*Fig. 3**Fig. 4**Fig. 5*

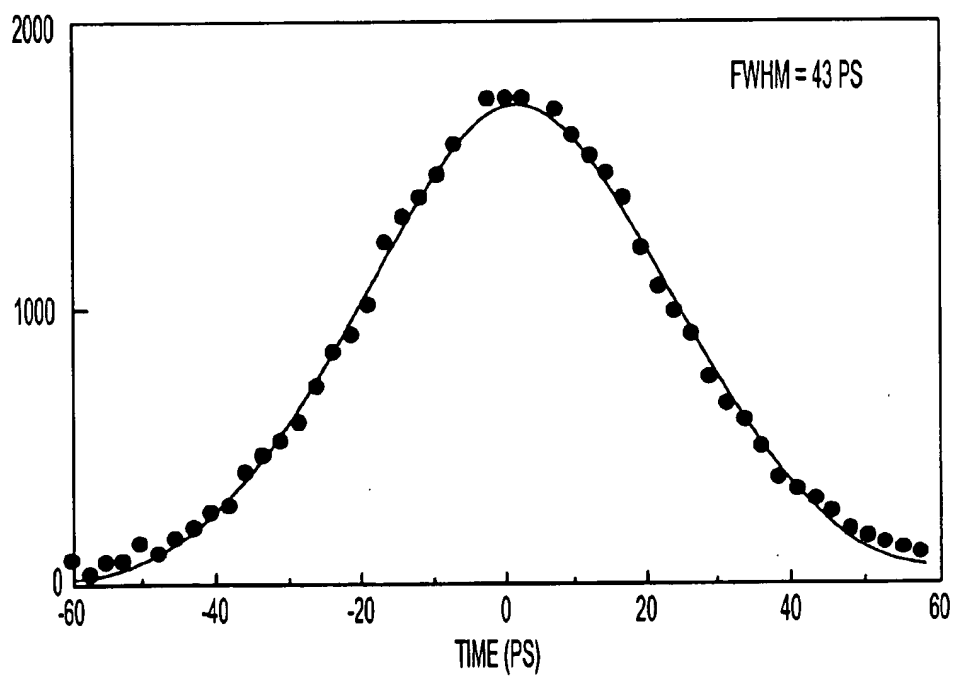
*Fig. 6**Fig. 7*

*Fig. 8**Fig. 9*

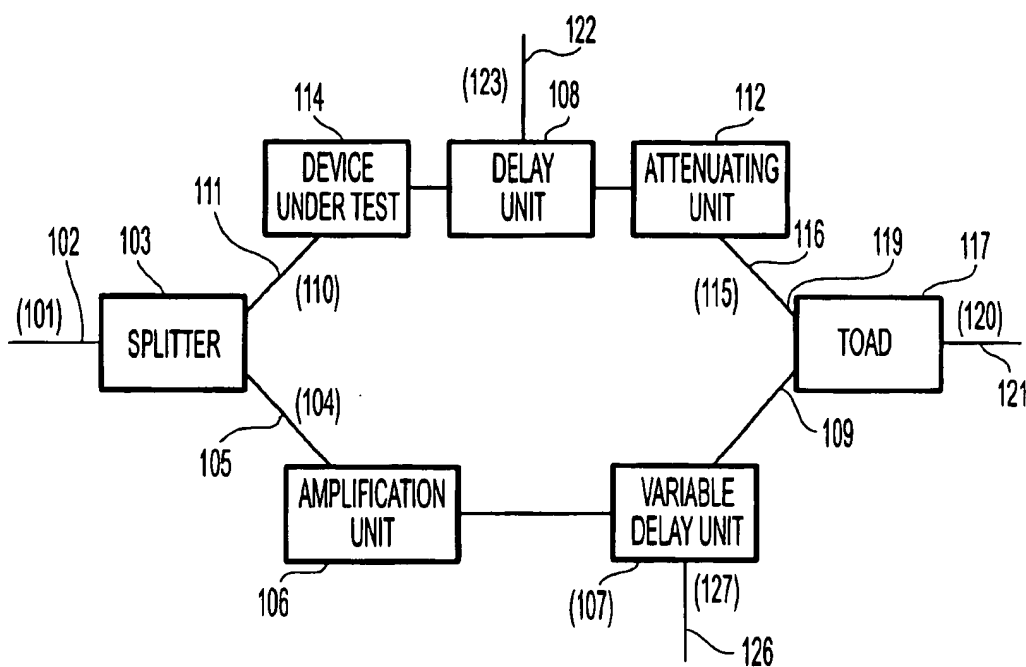
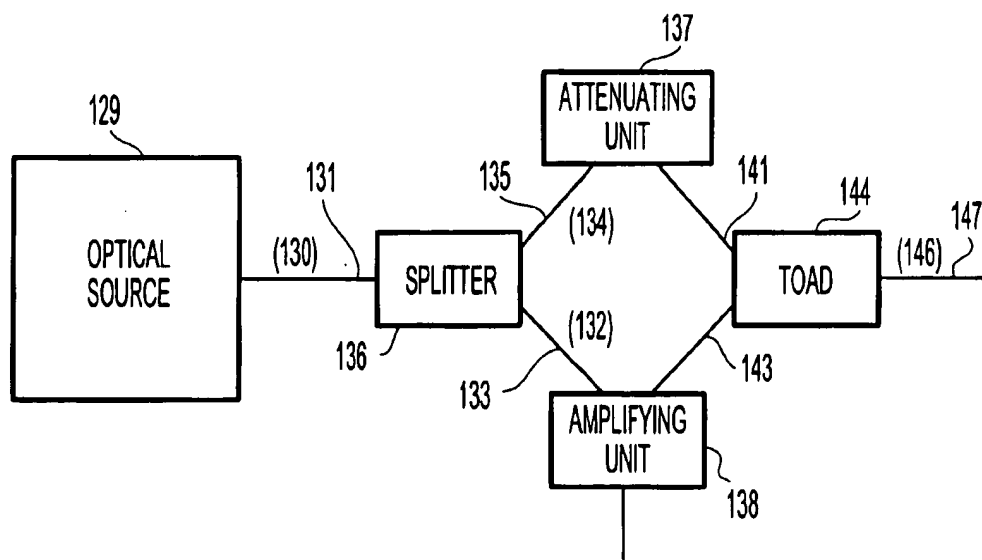


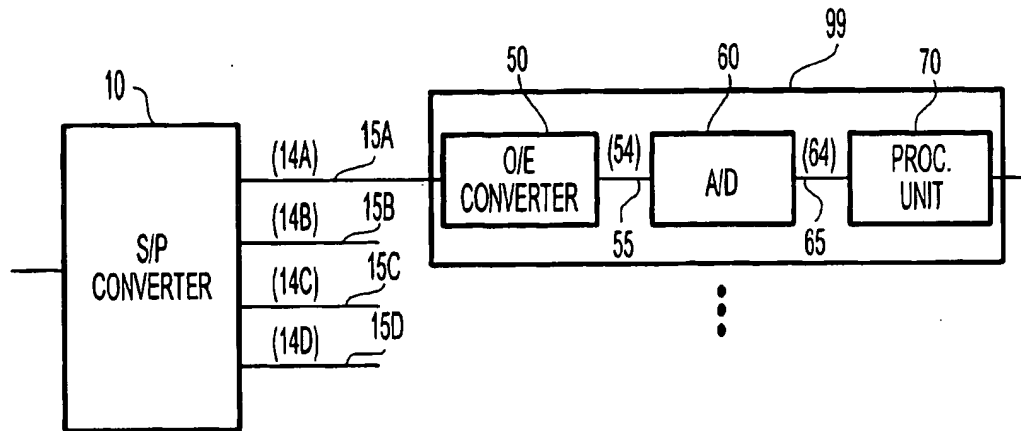
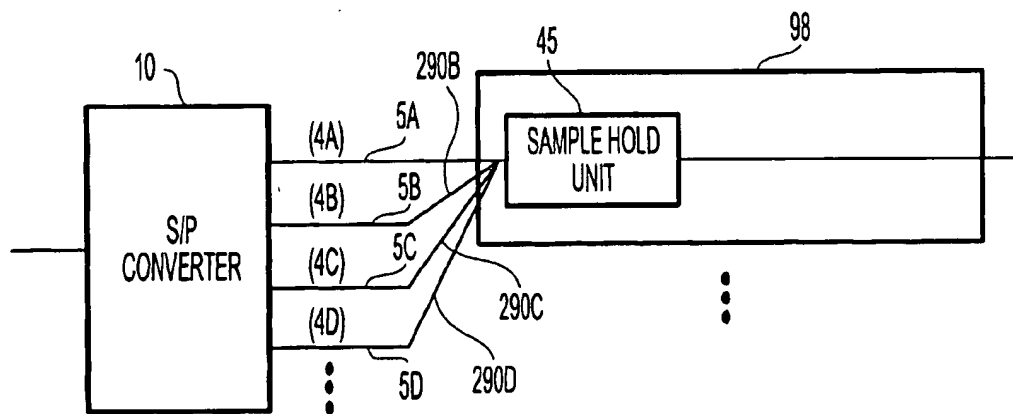


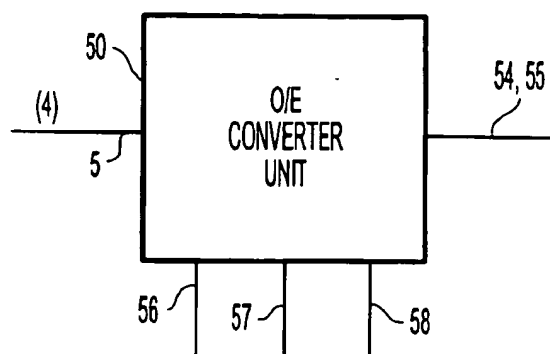
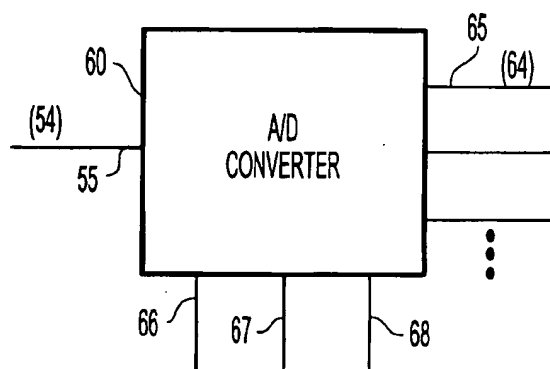
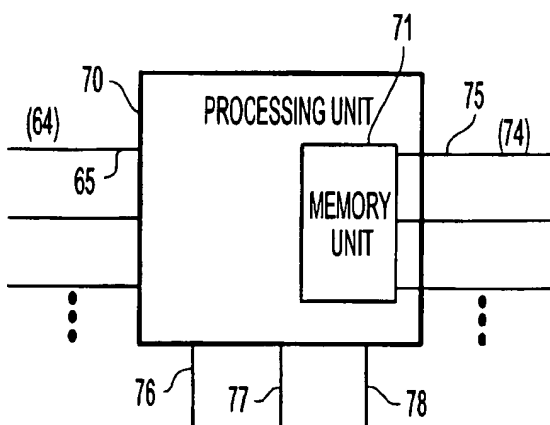
*Fig. 10*  
*Prior Art*



*Fig. 11*

*Fig. 12**Fig. 13*

*Fig. 14**Fig. 15*

*Fig. 16**Fig. 17**Fig. 18*

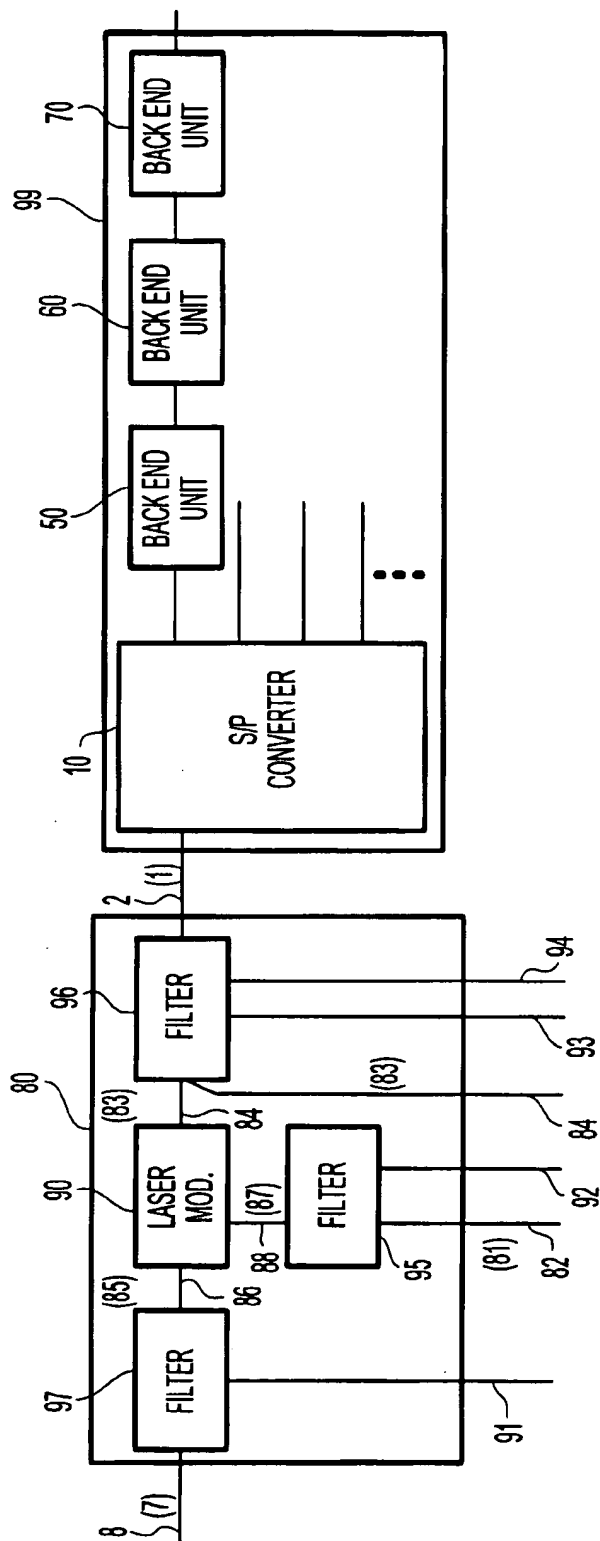


Fig. 19

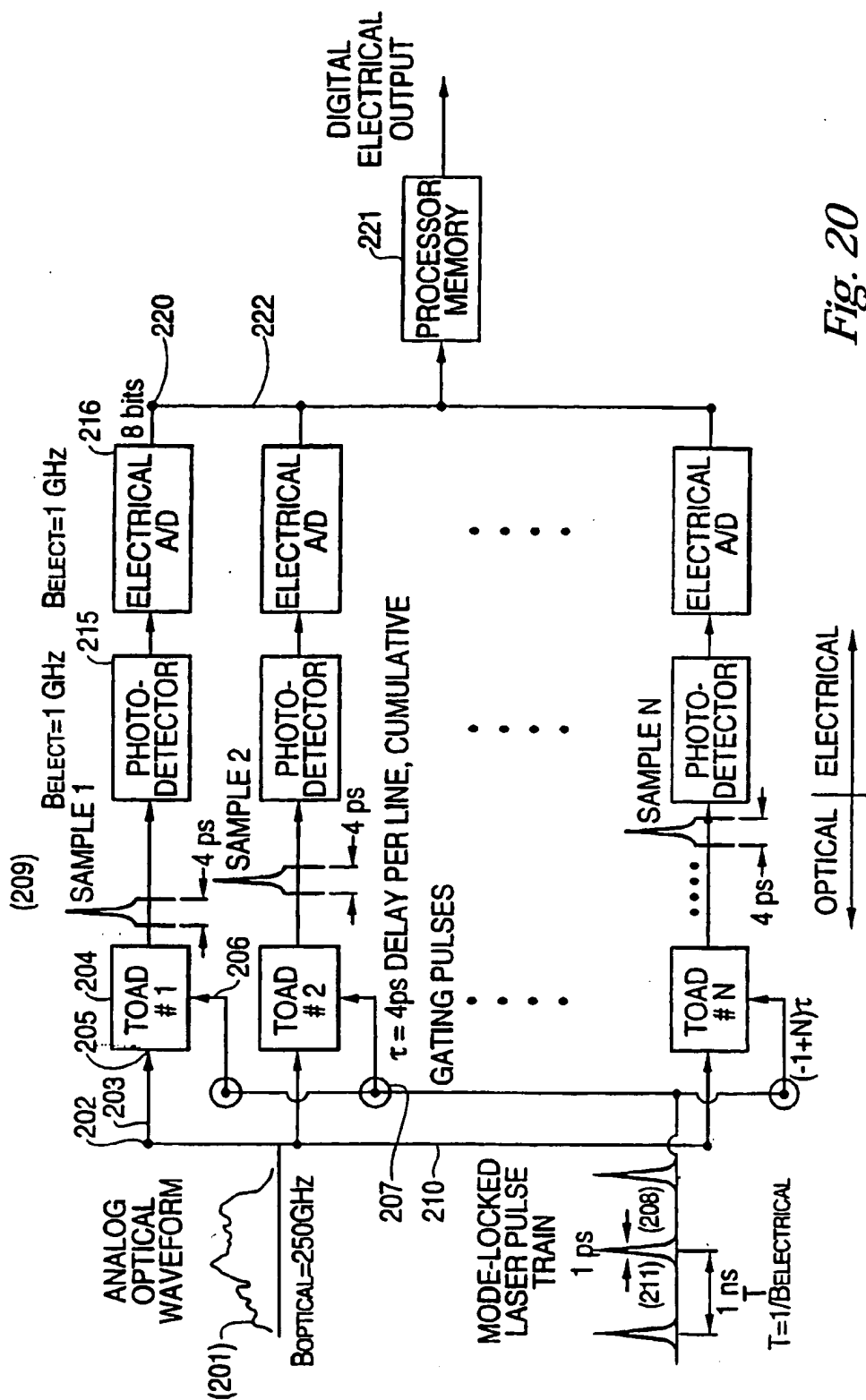


Fig. 20

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## HIGH-SPEED SERIAL-TO-PARALLEL AND ANALOG-TO-DIGITAL CONVERSION

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates generally to the field of optoelectronic devices and, more particularly, to devices which function as extremely high speed optical shutters, and to applications of such devices.

#### 2. Description of the Related Art

A number of important commercial, scientific, medical and military signal processing or sampling applications require high speed conversion of time-varying analog waveforms into digital form. Such higher digitization speed is useful because, among other reasons, it provides better spatial resolution for lidar and range-finding, better time resolution for clock synchronization protocols, better instrumental resolution for sampling oscilloscopes, and better channel separation for wideband receivers. Higher speed analog-to-digital (A/D) converters are additionally sought because there is often a threshold conversion rate below which the application requiring the samples is infeasible, such as digital receivers operating in a particular microwave band.

It is known that an analog serial-to-parallel (S/P) converter can be used to parcel out portions of a time-varying waveform to parallel A/D converters working in parallel. In such systems, the quality of the S/P converter stage bounds the subsequent fidelity of the overall converter, so manufacturability and control of noise are crucial considerations. Unfortunately, today's all-electronic S/P converters operate well below 60 gigasamples per second (GSPS), which is not much faster than today's state-of-the-art electronic A/D converters (e.g., 6 GSPS claimed by Rockwell in the laboratory, for which, to applicants' knowledge, no publicly-available enabling disclosure exists), so there is little fan-out by the S/P converter. By way of comparison, all-optical switching/sampling phenomena can occur at intrinsically higher speeds than analogous electronic phenomena, since electron mobility in the solid state is up to 10,000-fold slower than the speed of light; the advantage is lessened by the ratio of device sizes.

### SUMMARY OF THE INVENTION

Accordingly, it is among the objects of the instant invention to provide one or more of the following: (i) an improved A/D converter operating at optical speeds yet benefiting from progress in the speed of electronic devices; (ii) an integrated, fast A/D converter; (iii) an improved A/D converter with calibrated outputs and servo-controlled input range; (iv) an improved A/D converter with a parallel output signal; (v) an improved A/D converter in a circuit; (vi) an A/D converter embedding a fast analog S/P converter; (vii) an integrated fast analog S/P converter; (viii) a fast analog optical S/P converter employing a TOAD (as defined below); (ix) an improved, fast analog S/P converter with adjustable input dynamic range; (x) an improved S/P converter with physical clocking; and (xi) a device capable of converting an optical waveform into piecewise portions employing a TOAD.

In accordance with these and other objects, there is provided an analog-to-digital converter, which includes a first input port configured to receive an analog optical waveform. The converter also includes a splitter connected to the first input port and configured to split the analog

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optical waveform into a plurality of identical waveforms. The converter further includes a second input port configured to receive a clock signal having a predetermined clock period. The converter also includes a delay circuit configured to receive the clock signal and to output a plurality of delayed clock signals each having different a different delay with respect to others of the delayed clock signals. The converter still further includes a plurality of optical shutters configured to respectively receive the plurality of identical waveforms on an input port thereof, and configured to receive a corresponding one of the plurality of delayed clock signals on a control port thereof, each of the plurality of optical shutters having an output port for outputting the corresponding one of the identical waveforms within a time period in a range of 0.01 psec to 100 psec. The converter also includes a plurality of photodetectors respectively connected to the output ports of the plurality of optical shutters and configured to convert an input optical signal into an output electrical signal. The converter further includes a plurality of electrical analog-to-digital converters respectively connected to the output ports of the plurality of optical shutters and configured to perform an analog-to-digital conversion of the corresponding electrical signal into a digital signal. The number of electrical analog-to-digital converters in a fully populated configuration is such that a conversion time of said analog-to-digital converters divided by the number of electrical analog-to-digital converters is slightly less than the time period of the optical shutters.

Aspects of the system and method according to the invention exploit and improve upon recent advances in high speed optical shutter technology, notably the Terahertz Optical Asymmetric Demultiplexer (TOAD), disclosed in U.S. Pat. No. 5,493,433, which is incorporated in its entirety herein by reference. Whereas most optical shutters require impractically long interaction lengths, high power, or both; the TOAD is compact and low power.

The TOAD exploits a strongly non-linear optical effect which allows a gating pulse to cause either 0 or  $\pi$  radians of phase delay in a signal introduced into an interferometer. The phase delay switches off after a brief interval, of the order of 1 picosecond (psec), so a signal beam meeting with itself in a TOAD interferometer will emit only the waveform sampled by the 1 psec shutter window. In contrast to conventional semiconductor logic gates, the TOAD does not try to switch and reset in a small multiple of the shutter cycle time. Rather, the TOAD can undergo an Open/Off cycle only once before it needs to recover, typically for 100 psec. When combined with a precise optical delay line, each TOAD can be used to sample (read) or inject (write) a signal's amplitude or intensity in the shutter window time. The TOAD is then latent, waiting for the electronics to invoke it again (e.g. every 4 nanoseconds (nsec) for 250 MHz CMOS).

Utilizing such high speed optical shutters, in accordance with the system and method according to the invention, it is possible to provide high speed, high quality S/P conversion, and therefore high speed A/D converter systems embedding a fast analog optical S/P converter with fan-out to whatever degree is necessary to support operation beyond 1000 gigasamples per second (GSPS). Also, in accordance with the invention, systems may include all-electrical A/D converter devices, thus providing a back-end with optimal price/performance. Preferably, the balance between more fan-out in the S/P converter and more, lower-cost slow electrical A/D converters in the back-end is optimally selected, based upon overall price, performance, manufacturability, or other criteria. While the present invention may be, and preferably is, practiced using the TOAD,

the concepts, teachings, and applications described herein below are by no means limited to TOAD-based systems, and will work with other optical shutters, other sequences of functional units, and with novel electrical A/D converters.

In accordance with the invention, the TOADs will preferably be solid state and formed by mass production processes. For instance, integrated semiconductor optical amplifiers (SOAs) under development at Princeton University, British Telecom, NEC, and elsewhere can be combined with integrated optical paths to form complete TOAD devices. SOAs can advantageously be formed using materials from columns III and V in the periodic table (e.g. GaAs), or II-VI materials; a plurality of optical paths can be formed on a low cost substrate; and the two monolithic constructions bonded together. Additionally or alternatively, a plurality of optical paths may be formed on the same substrate as the TOADs by additive, subtractive, or even selective phase-change direct-write processes. One may apply light, charged particle beam, heat, or other known methods to cure the waveguide material or optical interconnects.

In accordance with a preferred embodiment of the instant invention, the time-varying magnitude of an input signal is modulated by amplitude or intensity. In more general embodiments, modulation of the magnitude comprises a combination of amplitude modulation, polarization modulation, phase modulation, and frequency modulation. These can all be exploited in their own right by appropriate TOAD embodiments, or reduced to amplitude or intensity modulation and treated as in the preferred embodiment. For instance, a polarized signal can be converted into an intensity modulated signal by being passed through a cross-polarizer. A frequency modulated signal can be converted into an amplitude modulated signal in a number of ways, including filtering with a color-sensitive transmitter or reflector; or diffracting or refracting and then using position, time of flight, or phase information. A frequency modulated signal can be converted into an intensity modulated signal by interfering it with a coherent reference beam of comparable intensity and sampling the beat frequency. In general, modulation can be permitted to occur within the TOAD, instead of just prior to it. For instance, a phase modulated signal can be converted into an intensity modulated signal by being superposed on a coherent reference signal of comparable intensity within the TOAD interferometer itself, thus replacing the input splitter described in the '433 patent with a bypass on one side and a reference beam for differential measurement on the other side. This brief description is exemplary and not comprehensive. As those skilled in the art will appreciate, other methods are known, and it is anticipated that there will be future embodiments of optical shutters which will be appropriate for use in this invention.

#### BRIEF DESCRIPTION OF THE FIGURES

Various aspects, features, applications, and advantages of the instant invention are depicted in the accompanying set of drawings, which are intended to be exemplary and not limiting or exhaustive, and in which, briefly stated:

FIG. 1 illustrates a preferred embodiment of an analog optical S/P converter in block form.

FIG. 2 illustrates an analog optical S/P converter in greater detail.

FIG. 3 illustrates a beam splitter used in a clocking source.

FIG. 4 illustrates a clocking source including a modulator unit.

FIG. 5 illustrates a "physically clocked" embodiment of a clocking source.

FIG. 6 illustrate the use of delay lines to retard clock signals.

FIG. 7 illustrate the use of delay lines to retard data signals.

FIG. 8 illustrates an optical shutter unit implemented in a Terahertz Optical Asymmetric Demultiplexer.

FIG. 9 shows a measured TOAD waveform.

FIG. 10 plots the shape of a fast analog waveform using an optical correlator.

FIG. 11 shows a measurement of the same analog signal by a TOAD acting as an optical shutter.

FIG. 12 illustrates an apparatus in the manner of a sampling oscilloscope.

FIG. 13 illustrates a sampling oscilloscope using a TOAD acting as an optical shutter.

FIG. 14 illustrates an optical AID converter system embedding an analog optical S/P converter.

FIG. 15 illustrates an alternative embodiment of the slow AID converter back-end.

FIG. 16 illustrates a preferred slow O/E converter unit.

FIG. 17 illustrates a preferred slow electrical A/D converter unit.

FIG. 18 illustrates a preferred processing unit.

FIG. 19 illustrates an A/D converter system with analog electrical input and digital electrical output.

FIG. 20 summarizes an alternative A/D converter embodiment.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

Reference is now made to FIG. 1, which illustrates a preferred embodiment of an analog optical S/P converter in block form. Optical input signal (1) enters an optical S/P converter (10) by means of an optical path (2). Signal (1) is preferably coherent light, such as 1.5  $\mu\text{m}$  light, and comprises a waveform, such as shown in FIG. 9. Preferably, but not necessarily, signal (1) has already been amplitude or intensity modulated with certain data of interest. Path (2) is preferably an integrated waveguide, although a variety of designs for optical paths through free-space and guided paths (e.g. optical fibers) can be substituted, as would be appreciated by persons skilled in the art, e.g., optical engineers.

A plurality of output signals emerge from S/P converter (10), illustrated as signal (4A) on path (5A), signal (4B) on path (5B), and so forth. The reader should interpret references to "signal (4)" without a suffix as applying to a plurality of (4A), (4B), etc., and similarly with "path (5)" as applying to paths (5A), (5B), etc. Output signals (4) contain information from the input signal (1), and are preferably optical replicas of input signal (1), although a plurality of them may be scaled to different amplitudes from the input signal (1) and/or from each other. Optionally, output signals (4) may comprise functional modifications of input signal (1), such as linearization corrections, and/or may mix in other signal streams, such as a monochromatic reference beam.

Reference is now made to FIG. 2, which illustrates an optical analog S/P converter in greater detail. In this embodiment, a beam splitter (12) replicates an input signal (1) into a plurality of output signals (14), which exit on their optical paths (15). As persons skilled in the art will appreciate, one can purchase beam splitters with high uniformity and low parasitic losses commercially from a num-



ber of vendors, and beam splitters can also be integrated with optical or optoelectronic subsystems using well-known lithographic or casting techniques.

Each of a plurality of optical shutters (40) is fed both by a signal (14) along an optical path (15) from the beam splitter (12) and also by a clock signal (32) carried by an optical path (31). Each optical shutter (40) emits an output signal (4) on a path (5).

Clock signals (32) are illustrated schematically as originating from a single clocking source (20), but use of multiple clocking sources is permissible. The signal path (17) output of the input master clock (20) is used to synchronize the electrical A/D stages and subsequent latching circuitry.

Reference is now made to FIG. 3, which illustrates a beam splitter (30) used in a clocking source (20). In this embodiment, a master clock signal (28) of periodic pulses is introduced along path (29) and distributed as clock signals (32) among paths (31). Optionally, output clock signals (32) may comprise functional modifications of master clock signal (28), for instance by pulse-sharpening, clock-doubling, or polarization. Other signals may optionally be mixed in with output clock signals (32), such as complex waveforms. As one skilled in the art will appreciate, a number of clock distribution topologies are known to electronics engineers, with different topologies appropriate for different embodiments, such as a star-of-stars hierarchy for obtaining sufficient fan-out with tight timing synchrony. Some of these topologies also include an amplification unit within the clocking source (20).

Reference is now made to FIG. 4, which illustrates a clocking source (20) including a modulator unit (24) providing an optical signal (25) along optical path (26) to a beam splitter (30). A light signal (27) input from path (29) is preferably constant brightness from a coherent laser. The beam splitter could preferably be similar to the one illustrated in FIG. 3. If the modulator (24) is electro-optical, then it will preferably be fed by an RF electrical trigger signal (21) from an RF input path (22). If the modulator unit (24) is optoelectronic, then it will preferably be fed by an optical trigger signal (21) from an optical input path (22). Mixtures of electrical and optical inputs may also be imposed as a trigger signal (21) along a suitable plurality of paths (22).

Modulator unit (24) may require a power source, but such sources are well known to those skilled in the art, and are not depicted in the drawings in order to avoid distracting from the description of the present invention.

Reference is now made to FIG. 5, which illustrates a "physically clocked" embodiment of a clocking source. Use of a beam splitter with one-more-than- $2^N$  outputs is preferred, but not required. The function of modulator (24) in this embodiment is to convert a "flyback" trigger signal (35) into a suitable input for beam splitter (30), preferably by amplification and pulse-sharpening, so that a preferred clocking source (20) emits clocking waveforms (e.g., pulses) in parallel at precise periodic intervals that do not depend on the coherence of an external clock. An optical clock signal (32C) is provided by optical path (31C) to optional phase correction unit (33), which emits signal (35) after that time interval necessary to ensure that the periodicity of pulses arriving at beam splitter (30) is a constant. There can be one or a number of pulses in transit traversing the circuit encompassing (34), (24), (26), (30), (32), and optionally (33); the circuit serves as a delay line. If optional phase correction unit (33) is omitted, path (31C) and path (34) number the same item.

The optional phase correction unit (33) can serve to adjust the timing of the arrival of clock signal (35) at modulator unit (24), and can be internally controlled by a clock or externally controlled along a path (37), such as by "trimming" feedback from elsewhere in the S/P converter or a system embedding it. A number of units for phase correction are well-known, including stretching optical fibers and tight temperature control.

A starting signal is used for the clocking source (20), and the clocking can run thereafter without requiring an external clock. There are a number of units for providing a starting signal. An optional input (36) may be provided through phase correction unit (33) or directly into modulator unit (24) to provide a pulse from outside as the starting signal; or, the starting signal can be generated internally, for instance by compounding its amplification through repeated cycles until effective.

Reference is now made to FIG. 2, FIG. 6 and FIG. 7, which illustrate the use of delay lines to relate the relative timing of clock signals (32) and signal waveforms (4). Note that an optical path length is determined by a path's index of refraction as well as its physical length. In the embodiment shown in FIG. 6, the optical lengths of the signal paths (15) are all the same, but each clock path (31A), (31B), (31C), and so forth has an optical length chosen to provide timing delays in successive integer units of  $\tau$ . In an alternative embodiment shown in FIG. 7, the optical lengths of the clock paths (31) are all the same, but each signal path (15A), (15B), (15C), and so forth has an optical length chosen to provide timing delays in successive integer units of  $\tau$ . More complicated patterns can be utilized while remaining within the scope of the invention as described herein. For example, in embodiments of most value in certain applications, manufacturability considerations make it preferable for the ensemble of clock signals (32) and the ensemble of waveforms (14) to intersect at a variety of times and places, in a matrix-like configuration (e.g., clustered on chips in a module). Nor must the intersections be regular; in some embodiments for applications described below, they need not all have the same time intervals  $\tau$ , nor comprehensive coverage, nor sequential ordering.

Reference is now made to FIG. 8, which illustrates an optical shutter unit (40) implemented in a TOAD, such as the Mach-Zehnder version disclosed in the '433 patent. Optical shutters can also be built using an amplitude-modulating TOAD constructed from a Mach-Zehnder, Michelson, or Sagnac interferometer by means of techniques well-known to those ordinarily skilled in the art. There have been attempts to build a TOAD using a loop mirror. These and other forms of TOAD are all appropriate for use as optical shutter units in connection with the instant invention, where each embodiment of an optical shutter (40) is preferably a TOAD (41) which gates a time-dependent input signal (14) with its time-dependent waveform (42) to an output signal (4) with a modulated magnitude.

Referring now to FIG. 8, the Terahertz Optical Asymmetric Demultiplexer (TOAD) comprises a fiber or waveguide loop joined at its base by the top half of a symmetric 2x2 splitter (18). The bottom side of the splitter (18) receives the signal input and transmits it to a photodetector at a receiver. In general operation, light from the input is split by the splitter into two identical waveforms which travel through the loop in opposing directions. Because the two signal components will have traversed exactly the same distance when they meet again in the splitter (18), purely constructive interference occurs; the splitter (18) therefore reflects all light back out the original input fiber and passes no light to

the detector. This loop-mirror also contains a nonlinear element (e.g. a semiconductor optical amplifier (SOA)) located slightly off-center from the midway point. The asymmetric placement is the reason for the letter "A" in the word TOAD.

If injected into the loop before the signal pulse, a clock or pulse will change the nonlinear element's index of refraction for a brief period of time (the dwell time). This means that the light traversing the loop after the gating pulse has passed through the SOA will encounter a different propagation delay than light traversing the loop before the gating pulse pumped the SOA. An important feature of the TOAD is that this delay is engineered to be exactly one-half of a wavelength, or exactly enough to change the interference condition from constructive to destructive. The coupler therefore expels light to the photodetector instead of back out the input.

In accordance with Nyquist's Theorem, for a system with maximum frequency component  $2/\tau$ , no information is available about the shape (roughly speaking,  $\sigma$ ) of the shutter waveform so long as  $\sigma < \tau$ . In practice, the shutter waveform (32) has a finite rise time and fall time, so cross talk is reduced significantly but not eliminated by making  $\sigma$  somewhat smaller than  $\tau$  (e.g. 50%).

Reference is now made to FIG. 9, which shows a measured TOAD waveform; in this case, 4 psec wide. The measurement was made by duplicating the output of a single TOAD device, delaying the second waveform by a variable interval (shown as the abscissa) and measuring the amplitude of the convolution of the first against the second (shown as the ordinate). The delay was swept from 0 to 10 psec and the results plotted.

Reference is now made to FIG. 10, which plots the shape (44) of a fast analog waveform (actually, a laser pulse) as measured in the standard way by an optical correlator. FIG. 10 is prior art.

Reference is now made to FIG. 11, which shows a measurement of the same analog signal by a TOAD acting as an optical shutter (41) in the manner of FIG. 9. The measurement was performed in the inventor's laboratory by creating a rudimentary sampling oscilloscope using approximately 43 psec-wide pulses from a 1.3  $\mu\text{m}$  wavelength laser. The repetition rate was chosen as 10 nsec so that the output of the TOAD could be measured with a 100 MHz photodetector. The clocking train was shortened to 1 psec wide pulses at 500 femtojoules of energy per pulse, and was injected into the control port of the TOAD as gating pulses. A weaker branch of the same train was split from the first, acting as the lower amplitude signal to be measured, and was time-lagged along a precisely varied delay path before being injected into the input port of the TOAD as signal pulses. The delay path was then changed and the TOAD output measured again. The overall shape was obtained by sweeping the delay path of the signal relative to the control over a range of 100 psec. The FWHM  $\sigma_{\text{FWHM}} = 43$  psec, and the area under the curve corresponds to the intensity of the input signal integrated over the time when the TOAD acted as an open shutter. It is clear by inspection that the measurement provided at least 6 bits of resolution on the ordinate axis.

The practiced sampling oscilloscope method indicates a useful analog application of the TOAD. The embodied sampling oscilloscope apparatus proves an alternative embodiment of the S/P converter wherein the fan-out feeds a plurality of branches—in this example, 1—and the conversion is repeated temporally at precisely known phase offsets, not necessarily sequentially, in order to measure the

shape of a repeated signal. The signal must be reproducible in a finite time domain. A number of means for reproducible signal delay lines with sub-psec precision are known and could have been used instead to create the densely sampled phase offsets. Reference is now made to FIG. 12, which illustrates an apparatus in the manner of a sampling oscilloscope which relies upon analog data measured by a TOAD optical shutter. A coherent optical signal (101) is fed on optical path (102) to a splitter (103) which feeds an output signal (104) to optical path (105) and an output signal (110) to optical path (111). Signal (110) on optical path (111), even if weakened, enters device-under-test (114) and emerges as signal (115) on optical path (116). There may optionally be a plurality of amplifying units (106) along optical path (105); and/or there may optionally be a plurality of attenuating units (112) along the optical path traversing (103), (111), (114), and (116); in any case, at least one of these options must be implemented since the signal (115) must be weaker than the non-linear regime of the TOAD device (117) and signal (104) must be stronger than the switching threshold and must arrive at the input port (109) prior to the arrival of signal (115) at input port (119). The plurality of attenuation elements is depicted explicitly as a single unit (112) but could in practice be anywhere along said path, including merged with other units; likewise with the plurality of amplification units depicted as a single unit (106). There must also be a plurality of variable delay units (107) and/or (108) which introduce the phase offsets needed to sample the interval of interest. The control units can be internally controlled and/or externally controlled.

External control signal (127) would be introduced through path (126) and control signal (123) would be introduced through path (122). The TOAD (117) emits a signal (120) on optical path (121), said signal being representative of the convolution of the time aperture of optical shutter (117) with the amplitude of signal (115). Note that it is not strictly necessary for the elements mentioned—including the device-under-test, splitter, delay units, amplification units, attenuation units, and optical paths—to precisely preserve the color of signal (115) with respect to signal (104), since the clocking signal entering (109) is not interfered against the data signal (115) entering (119). Therefore, optical to-electrical and electrical-to-optical converters may be used advantageously in device-under-test (114).

Reference is now made to FIG. 13, which illustrates an alternative embodiment in the manner of a sampling oscilloscope which relies upon analog data measured by a TOAD optical shutter and uses the waveform being measured additionally as its own clock signal. An optical source (129), which may advantageously be an electrical-to-optical converter, introduces a signal (130) onto optical path (131). A splitter (136) divides the signal (130) into signal (134) on optical path (135) and signal (132) on optical path (133). The embodiment attenuates (137) and/or amplifies (138) the signal. There must be at least one variable delay unit (not depicted) along the upper or lower path, as in FIG. 12. The clock signal is required to arrive at port (143) before the data signal arrives at port (141). The TOAD (144) emits a signal (146) on optical path (147).

Other embodiments of sampling oscilloscopes are known in industry and their reimplementation with TOAD-based optical shutters would be self-evident for one ordinary skill in the art.

Reference is now made to FIG. 14, which illustrates an optical A/D converter system (99) embedding an analog optical S/P converter. Preferably, an O/E converter (50) accepts an optical signal (14) from each of the paths (15)

emitted from a S/P converter (10), and converts said optical signal into an electrical signal (54). An A/D converter (60) accepts the electrical signal (54) from electrical lines (55) and produces a digital electrical representation (64). The electrical lines are likely to be transmission lines implemented as wires for low-speed operation and microwave plumbing or coaxial paths for high speed operation. Optionally, a processing unit (70) accepts said digital electrical signal (64) along electrical lines (65) and delivers a corrected, buffered version. In an alternative embodiment, the A/D converter may incorporate the O/E converter integrally, so (54) and (55) would be omitted.

Reference is now made to FIG. 15, which illustrates an alternative embodiment of the slow A/D converter back-end: an all-optical A/D converter (98). An optical sample-and-hold unit (45) accepts the optical signal (4) from its optical path (5), and slowly digitizes it, such as by the method disclosed in U.S. Pat. No. 4,947,170, incorporated herein by reference. The optical signal (4) may comprise a waveform encompassing a plurality of copies provided to a common input line in time sequence. The time sequence can be constructed, for example, by merging optional delay lines (290) of differing lengths, with the delay lines originating from a common output of (10).

Reference is now made to FIG. 16, which illustrates a preferred O/E converter unit (50) for converting an analog optical signal (5) into an analog electrical signal (54) representative of it. Techniques for increasing the range and sensitivity and limiting the noise introduced by optical-to-electrical converters, such as photodetectors, are well-known. Common commercially available optical-to-electrical converters include avalanche photodetectors, photomultiplier tubes, charge-coupled devices, PIN junctions, photosensitive resistors, photovoltaic devices, and photosensitive capacitors, among others. Certain O/E converter implementations can advantageously be implemented with time-dependent control signals (56), such as a reset signal; with a powering unit (57); and/or with scaling unit (58), such as for dynamic range, bias and gain, linearity, or sensitivity settings, possibly entailing connections to other units in the system (not depicted). Each input path (5) may in fact comprise a plurality of optical paths, each carrying its own coded version of optical signal (4); each output path (55) may in fact comprise a plurality of electrical lines, each conveying its own coded electrical signal (54). The coding may be trivial (e.g. none) or complicated for reasons arising from fault tolerance, power reduction, noise reduction, and packaging, among others.

Reference is now made to FIG. 17, which illustrates a preferred A/D converter (60) for converting an analog electrical signal (54) into a digital electrical signal (64) representative of it. In general, each A/D converter requires a time-dependent control signal (66), preferably a clocking signal related to the clocking signal of its optical particular optical shutter (40). A time-dependent control signal will also be provided to its processing unit (70) in order to know when to latch the signal, and analog sample-and-hold units or digital latches may advantageously be added at other points in accordance with well-known engineering practices. Certain implementations of A/D converter (60) can advantageously be implemented with additional time-dependent control signals (66), such as a reset signal; with a powering unit (67); and/or with scaling unit (68), such as for dynamic range, bias and gain, linearity, or sensitivity settings, possibly entailing connections to other units in the system (not depicted). Each input path (55) may in fact comprise a plurality of electrical lines, each carrying its own coded

version of electrical signal (54); the coding may be trivial (e.g. none) or complicated for reasons arising from fault tolerance, power reduction, noise reduction, and packaging, among others. Each output path shown as (65) will generally comprise a multiplicity of electrical lines, each conveying its own coded electrical signal (64), where the coding will preferably be binary.

Reference is now made to FIG. 18, which illustrates a preferred processing unit (70) for converting a plurality of digital electrical signals (64) into a different plurality of electrical signals (74) representative of it. In the preferred embodiment, processing unit (70) is optional. A powering unit (77) will advantageously be required for (70). Certain implementations of processing unit (70) can advantageously be implemented with time-dependent control signals (76), such as a reset signal or output bus system clock signal; and/or with scaling unit (78), such as for dynamic range, bias and gain, linearity, or sensitivity settings, possibly entailing connections to other units in the system (not depicted). For each stage (70), custom calibrations can be measured through the individual path through (10), (40), and (50). The calibrations can be applied locally or later; a lookup table may advantageously be employed with or without calibration data using memory unit (71) in order to expedite remapping signals to appropriate (e.g. linear) representations of the original input waveform's magnitude at a given time. Examples of the other units in the system would be from an input stage to servo the dynamic range. Each input path (65) generally comprises a plurality of electrical lines, each carrying its own coded version of electrical signal (64). The coding may be trivial (e.g. none) or complicated for reasons arising from fault tolerance, power reduction, noise reduction, and packaging, among others.

In the preferred embodiment, the ensemble of electrical signals (74) will be buffered, latched, and clocked onto a system bus by way of lines (75), in which case a memory unit (71) is also provided for the processing unit (70). For this reason, the synchrony of presenting the ensemble of electrical signals (74) to a system bus restricts the architecture in which the processing unit (70) is implemented. Simple digital systems require a master clock which will advantageously be the cycle time of the flyback signal (35), so all the latched bits will be injected onto the system bus simultaneously. Such an embodiment produces a large current impulse  $dI/dt$ , hence large simultaneous switching noise which must be decoupled with a large, expensive capacitance between power and ground. More complicated but affordable digital systems splay the latched bits onto the bus over a distribution of time slots, reducing the requirement for decoupling capacitance in proportion to the increase in the rise time window,  $dt$ .

Each output path (75) will generally comprise a plurality of electrical lines, each conveying its own coded electrical signal (74), where the coding will advantageously be binary and optionally for error detection/correction. In alternative embodiments, the output path (75) may convey data other than binary electrical signals, such as multistate digital, accept/reject/don't\_care evaluations, alarms, acoustic signals, or mechanical action.

Reference is now made to FIG. 19, which illustrates an A/D converter system with analog electrical input and digital electrical output. Note that in the preferred embodiment, processing unit (70) is optional. In the preferred embodiment, an input stage (80) is implemented as a laser modulator (90), such as the module sold by United Technologies Photonics (UTP). Other input stages may be advantageous, such as the method and apparatus disclosed in

U.S. Pat. No. 4,681,449, incorporated in its entirety herein by reference. Laser modulator (90) receives an electrical input signal (7) and a constant, coherent light source (81); its output signal (83) is the modulation of light signal (81) by the amplitude or intensity of the electric input signal (7). It may be advantageous to embed the A/D converter system in other circuitry, including front-end circuitry, in order to enable applications described herein below.

The dynamic range of the TOAD devices (41) is finite, so rescaling the input signal that reaches the S/P converter (10) advantageously broadens the dynamic range of operation for the system comprising (10) and (99). Attenuation can avoid non-linear and time-dependent saturation effects while amplification can avoid a noise floor. In the preferred embodiment, an optional electrical filter (97) can be employed to bias, attenuate or amplify the electrical input signal (7) from a microwave guide (8) into electrical signal (85) along path (86). In the preferred embodiment, the electrical filter (97) is a dynamically variable voltage divider and traveling wave amplifier. In an alternative embodiment, an optional optical filter (95) optically amplifies or attenuates a constant coherent signal (81) from path (82) as signal (87) on path (88). In an additional alternative embodiment, an optional optical filter (96) optically amplifies or attenuates a time-varying optical signal (83) from path (84) as signal (1) on path (2). Note that path (84) is marked twice since it may advantageously be accessible from outside unit (80). For instance, if an optical input signal is available instead of an electrical input signal, the filter (96)-which is depicted as part of optional unit (80)-may still be advantageously employed as a front-end to the A/D converter system (99) without using electrical inputs. An optional reference beam (94) may also be fed into the system for various reasons, notably to convert a phase modulated signal (83) into an amplitude modulated signal (1), or to bias a signal (83).

Typically, a first control unit (not shown) would provide a first control signal (91) to filter (97), a second control unit (not shown) would provide a second control signal (92) to filter (95), and a third control unit (not shown) would provide a third control signal (93) to filter (96). The control unit would be set by the downstream processing unit (70); processing unit (70) may establish the need to set control signals (91), (92), and/or (93) from data reported to it by (78) from externally or from units (50), (60), or (80). It may be advantageous to servo the input filters (95), (96), and/or (97) and performance characteristics of the back-end units (50), (60), and/or (70), for instance to diagnose problems or optimize performance. Some, none or all of these optional filters and connections to (70) may be employed. In the absence of unit (97), electrical path (86) is electrical path (8), and electrical signal (85) is electrical signal (7). In the absence of unit (95), optical path (88) is optical path (82), and optical signal (87) is optical signal (81). In the absence of unit (96), optical path (2) is optical path (84), and optical signal (1) is optical signal (83).

Reference is now made to FIG. 20, which concisely depicts an alternative embodiment employing  $N=250$ -fold fan-out in the S/P converter, a 1 psec external clock waveform,  $\tau_{\text{TOAD}}=4$  psec TOAD apertures, and  $B_{\text{electrical}}=1$  GHz electronics to sample a  $B_{\text{optical}}=250$  GHz optical waveform at 250 GSPS. This embodiment synchronously distributes a high-speed serial data stream into a large number of low-speed parallel data streams. Slower data streams are photoconverted, then sampled by all-electrical A/D converters, and then latched into a memory unit.

An optical waveform (201) enters at the upper left-hand corner of the diagram. The optical waveform is distributed

N-ways by an optical splitter, where the fan-out N is given by  $N=B_{\text{optical}}/B_{\text{electrical}}$ . The larger the electrical bandwidth  $B_{\text{electrical}}$ , the smaller the requisite minimum size of the splitter. For example, if the optical (input) bandwidth were 20 GHz and the A/D converter leaf nodes each operated at 1 GHz, then at least a 20-way splitter would be required. The repetition rate of the mode-locked laser driving the system is chosen to correspond to the bandwidth of the electronics, that is,  $1/T=B_{\text{electrical}}=250$  GHz. Here, the fan-out is 250-fold by a star splitter hierarchy (202) into 250 equivalent taps, each feeding an equal length delay line (203) followed by a TOAD (204).

Each TOAD has two inputs, one for the signal (205) and one for the control or gating pulse (206). The gating pulses will cause the TOAD to open a 4 psec sampling window (209), allowing that portion of the analog waveform from the signal input to pass to the output of the TOAD and onward. The remainder of the analog waveform outside the 4 psec window is suppressed and does not pass to the output of the TOAD.

Each TOAD connects its gating input to a delay line (207) a unique distance from a mode-locked laser pulse source, most readily through a hierarchical clock distribution tree (210). Timing of the control pulses at each TOAD is staggered by a  $\tau_{\text{TOAD}}=4$  psec increment from its neighbors, so that the N samples produced at the outputs of the N adjacent TOADs monitor 4N psec. The N samples are taken during a time period  $T=N \tau_{\text{TOAD}}=N B_{\text{optical}}^{-1}/B_{\text{electrical}}$ . Some time later, when the N samples have been taken, the next mode-locked laser pulse (211) enters the array of TOADs and another series of N samples is taken. A continuous sample is composed piecewise as each TOAD takes a snapshot through its time-limited window on the waveform, shoulder to shoulder with the other TOADS. In this way the sampling of the analog waveform continues round-robin without interruption. In practice, the repetition rate of mode-locked lasers can be from kHz to THz.

The pulse energy required after the splitter is approximately 500 femtojoules. This is readily achieved by using a conventional Nd:YLF laser if  $N<100$ . Here, with  $N=250$ , an amplified mode-locked fiber ring laser or a mode-locked semiconductor laser may be used. If insufficient power is available from the laser, then several lasers may be synchronously mode-locked.

Note that timing jitter within the A/D is negligible: arbitrarily smaller than the Nyquist limit. The lengths of the (fiber optic or solid state waveguide) delay lines are set at manufacturing time and can be compensated for foreseeable or measurable variations in temperature, humidity, vibration, or voltage supply. The system's spurious free dynamic range will therefore be limited by drift in the timing of the externally supplied control pulse and should preferably exceed 120 dB within the A/D module.

The timing control pulse can be physically clocked as in FIG. 5 with a precision well below the Nyquist limit, leaving no measurable jitter within the specified operating rate.

Each of the TOADs then feeds a dedicated photoconverter (215) (e.g. a semiconductor avalanche photodiode or PIN junction, depending on energetics). Note that the photodetectors under consideration can be filled at any rate (e.g. over 1 psec or 1  $\mu$ sec) and can recover faster than the A/D converters (216) they feed, so final low-cost A/D conversion remains the rate-limiting event.

The output is subsequently electrical, and is digitized by each A/D converter (216) at, for example, 1 GSPS with 8-bit resolution. The 1 GHz cycle time is sufficiently slow that the

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photodetector and A/D converter electronics can respond and recover completely and be ready for the next sample.

In the preferred embodiment, local control logic (220) remaps each A/D converter's output channel against a calibration table to ensure linearity, and then either stores the data (221) for later downloading at leisure, or else writes the electrical data to a very wide synchronous bus (222). The bus (222) does not need to operate at the same speed as the (rate-limiting) A/D converters (216), and making the bus (222) faster or reading a slower input signal would permit the bus (222) to be proportionately narrower.

While the foregoing description has touched upon various preferred embodiments and applications of the instant invention, those skilled in the art, having read the foregoing, will immediately recognize that the concepts detailed therein can be implemented and/or used in numerous obvious alternative structures and applications. Accordingly, it is understood that the scope of applicants' invention shall not be limited to those preferred and/or exemplary embodiments described herein, but instead, shall be defined exclusively by the finally-issued claims (which claims are intended to be read in the broadest reasonable manner), and any and all equivalents thereto.

What is claimed is:

1. An optical-to-electronic converter, comprising:

an input port, which receives an optical signal that is to be sampled;

an optical sampler stage including at least one high-speed optical shutter, which samples the optical signal at a first sampling rate by opening and closing the at least one high-speed optical shutter and which provides a plurality of sampled optical signals as a result thereof, the optical sampler stage including a plurality of parallel channels, each different channel providing a different one of said plurality of sampled optical signals, the optical sampler stage including a splitter for splitting the optical signal into a plurality of identical optical signals prior to the sampling at the first sampling rate; and

an electronic analog-to-digital converter stage, which converts the plurality of sampled output signals into a plurality of digital signals, the electronic analog-to-digital converter stage performing the converting at a second sampling rate slower than the first sampling rate.

2. The optical-to-electronic converter as recited in claim 1, wherein the electronic analog-to-digital converter stage comprises a single analog to digital converter which receives the outputs from each of the plurality of parallel channels in a time sequential manner.

3. The optical-to-electronic converter as recited in claim 1, wherein the electronic analog-to-digital converter stage comprises a plurality of electronic converters disposed in a plurality of parallel channels, wherein the plurality of channels of the electronic analog to digital converter stage respectively receive the sampled optical signals output from the plurality of parallel channels of the optical sampler stage.

4. The optical-to-electronic converter as recited in claim 1, further comprising a conversion stage disposed between the optical sampler stage and the electronic analog-to-digital converter stage, the conversion stage performing a conversion of the plurality of sampled optical signals into a plurality of electronic sampled signals.

5. The optical-to-electronic converter as recited in claim 4, wherein the conversion stage includes a plurality of photodetectors respectively disposed in the plurality of parallel channels of the optical sampler stage.

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6. The optical-to-electronic converter as recited in claim 5, wherein the optical sampler stage comprises:

a plurality of terahertz optical asymmetric demultiplexer assemblies (TOADs) respectively disposed in the plurality of parallel channels of the optical sampler stage and each configured to sample a corresponding one of the plurality of identical optical signals at different times,

wherein the plurality of detectors are respectively disposed between the plurality of TOADs and the electronic analog-to-digital converter stage.

7. The optical-to-electronic converter as recited in claim 3, wherein the plurality of parallel channels of the optical sampler stage corresponds in number to n, and

wherein n multiplied by the second sampling rate is approximately equal to the first sampling rate.

8. An optical to electronic converter, comprising:

a first input port configured to receive an analog optical waveform;

a splitter connected to the first input port and configured to split the analog optical waveform into a plurality of approximately identical waveforms;

a second input port configured to receive a clock signal having a predetermined clock period;

a delay circuit configured to receive the clock signal and to output a plurality of delayed clock signals each having a different delay with respect to other of the delayed clock signals;

a plurality of terahertz optical asymmetric demultiplexer configured to respectively receive the plurality of approximately identical waveforms on an input port thereof, and configured to receive a corresponding one of the plurality of delayed clock signals on a control port thereof, each of the plurality of terahertz optical asymmetric demultiplexers having an output port for outputting the corresponding one of the plurality of approximately identical waveforms within a fixed time period;

a plurality of photodetectors, each different photodetector connected to a different one of said output ports of the plurality of terahertz optical asymmetric demultiplexers and configured to convert an input optical signal into an output electrical signal; and

a plurality of electrical analog-to-digital converters respectively connected to the output ports of the plurality of terahertz optical asymmetric demultiplexers and configured to perform an analog-to-digital conversion of the corresponding electrical signal into a digital signal,

wherein a number corresponding to said plurality of electrical analog-to-digital converters is a value such that a conversion time of the plurality of electrical analog-to-digital converters divided by the number of said plurality of electrical analog-to-digital converters is approximately equal to the time period of the plurality of terahertz optical asymmetric demultiplexers.

9. A method of optical sampling, comprising the steps of: receiving an optical signal that is to be sampled;

splitting the received optical signal into a plurality of approximately identical optical signals; and

respectively providing the approximately identical optical signals to a plurality of channels of an optical stage; and sampling, at the optical stage, the optical signal at a first sampling rate by opening and closing a high-speed

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optical shutter and providing a plurality of sampled optical signals as a result thereof, each of the plurality of parallel channels of the optical stage providing a different one of said plurality of optical signals.

10. The method as recited in claim 9, further comprising the step of converting the plurality of sampled optical signals into a plurality of electrical sampled signals.

11. An analog optical sampler, comprising:

a first input port that is capable of receiving an analog optical waveform that is to be sampled;  
a second input port that is capable of receiving a clock signal;

at least one Terahertz Optical Asymmetric Demultiplexer (TOAD) that is configured to receive the analog optical waveform and the clock signal; and

an output port, from which is output a sample of the analog optical waveform, the sample being provided to the output port based on an output of at least one TOAD;

wherein the analog optical waveform is sampled when said TOAD is triggered by the clock signal.

12. The analog optical sampler as recited in claim 11, wherein at least one of the first input port, the second input port, and the output port includes an optical waveguide or an optical fiber.

13. The analog optical sampler as recited in claim 12, wherein distinct polarizations or colors are used to multiplex the first and second input ports on a same optical waveguide or optical fiber.

14. The analog optical sampler as recited in claim 11, wherein the at least one TOAD includes a Mach-Zehnder interferometer.

15. An optical sampler system, comprising:

a first input port, which receives an optical analog waveform that is to be sampled;

a second input port, which receives an optical clock signal at a clock rate;

a plurality of optical samplers, which produce a plurality of sampled optical waveforms from said optical analog waveform at a rate dependent on said clock signal, at least one of said plurality of optical samplers including a Terahertz Optical Asymmetric Demultiplexer (TOAD); and

a plurality of output ports, which output said plurality of sampled optical waveforms.

16. An optical sampler system, comprising:

a plurality of first input ports for receiving an optical analog waveform;

a plurality of second input ports for receiving an optical clock signal at a clock rate;

a plurality of optical sampler nodes for respectively producing a plurality of sampled optical waveforms from said optical analog waveform at a rate dependent on said clock signal;

a plurality of output ports for respectively outputting said plurality of sampled optical waveforms;

a first optical distribution network for replicating and delivering a plurality of copies of said optical clock signal; and

a second optical distribution network for replicating and delivering a plurality of copies of said optical analog waveform, said second optical distribution network including delay lines of differing optical lengths so as to provide each of said plurality of optical sampler

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nodes with a substantially unique timeslice of said analog optical waveform upon receipt of a corresponding one of said plurality of copies of said optical clock signal.

17. The optical sampler system as recited in claim 16, wherein said plurality of copies of said optical clock signal are delayed with respect to each other by a preset delay amount.

18. The optical sampler system as recited in claim 16, wherein at least one of said plurality of optical sampler nodes include at least one Terahertz Optical Asymmetric Demultiplexer.

19. The optical sampler system as recited in claim 16, further comprising an optical-to-electronic converter stage connected to at least one of said plurality of output ports, and configured to receive said sampled optical waveform and to convert said modulated optical waveform into an electronic waveform.

20. The optical sampler system as recited in claim 19, further comprising an analog-to-digital converter stage connected to said optical-to-electronic converter stage, and configured to convert said electronic waveform into a digital signal.

21. The optical sampler system as recited in claim 20, wherein said plurality of optical sampler nodes produce said plurality of sampled waveforms on a plurality of parallel channels, respectively, the plurality of parallel channels corresponding to  $n$  in number,  $n$  being an integer greater than one,

wherein  $n$  multiplied by a first sampling rate of the conversion by said plurality of optical sampler nodes is approximately equal to a second sampling rate of said analog-to-digital converter stage.

22. The optical sampler system as recited in claim 16, wherein distinct signal levels of at least one of said copies of said optical clock signal and said copies of said optical analog waveform through distinct paths in said first and second distribution networks are provided as correction signals used to correct a calibration of subsequent magnitude measurements of said optical sampler system.

23. An optical sampler system, comprising:

a plurality of high-speed optical shutters, each having a signal input port capable of receiving an optical input signal, a trigger input port capable of receiving an optical clock signal, and an output port;

a first optical distribution network, which receives an optical clock signal and delivers a corresponding optical clock signal to the trigger input port of each optical shutter; and

a second optical distribution network, which receives an optical analog waveform and delivers a corresponding optical analog waveform to the signal input port of each optical shutter;

wherein, for each optical shutter, the corresponding optical clock signal is synchronized with the corresponding optical analog waveform to open and close a gating window during which the optical shutter produces an optical waveform sample on its output port.

24. The optical sampler system of claim 23, wherein the high-speed optical shutter is a TOAD.

25. The optical sampler system of claim 23, wherein the high-speed optical shutter is open for a duration in the range from about 0.01 psec to about 100 psec.

26. The optical sampler system of claim 23, wherein the optical waveform sample produced by each optical shutter is substantially unique.

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27. The optical sampler system of claim 23, wherein the second optical distribution network comprises delay lines of differing optical lengths.

28. The optical sampler system of claim 23, wherein the first optical distribution network comprises delay lines of differing optical lengths.

29. The optical sampler system of claim 23, further comprising an optical-to-electronic converter stage connected to the output ports of the plurality of high-speed optical shutters.

30. The optical sampler system of claim 23, wherein the first and second optical distribution networks each include an optical path over which correction signals are provided to correct a calibration of subsequent magnitude measurements of the optical waveform samples.

31. A method of sampling an optical signal, comprising the steps of:

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receiving a continuous optical analog signal having an intensity that may be any value within two predetermined intensity limits;

receiving an optical triggering signal;

providing the continuous optical analog signal to an optical shutter;

providing the optical triggering signal to the optical shutter; and

outputting from the optical shutter, a discrete sample segment of the continuous optical analog signal.

32. The method of claim 31, wherein the optical shutter is a high-speed optical shutter.

33. The method of claim 32, wherein the high-speed optical shutter is a TOAD.

34. The method of claim 31, wherein the duration of the discrete sample segment is within a range of about 0.01 psec to about 100 psec.

\* \* \* \* \*



US006593871B1

(12) **United States Patent**  
**Miethig et al.**

(10) **Patent No.: US 6,593,871 B1**  
(45) **Date of Patent: Jul. 15, 2003**

(54) **AUTOMATIC A/D CONVERT POSITIONING  
CIRCUIT AND METHOD**

(56)

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(\*) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
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**ABSTRACT**

A circuit includes a programmable delay circuit to provide a sequence of delayed pulses, an A/D circuit to convert a sequence of values into digital values sampled at times defined by the sequence of delayed pulses, and a jitter correction circuit to adjust the programmable delay circuit based on a sequence of digital values from the A/D circuit sampled at times defined by the sequence of delayed pulses.

**20 Claims, 7 Drawing Sheets**

(21) Appl. No.: **09/942,688**

(22) Filed: **Aug. 31, 2001**

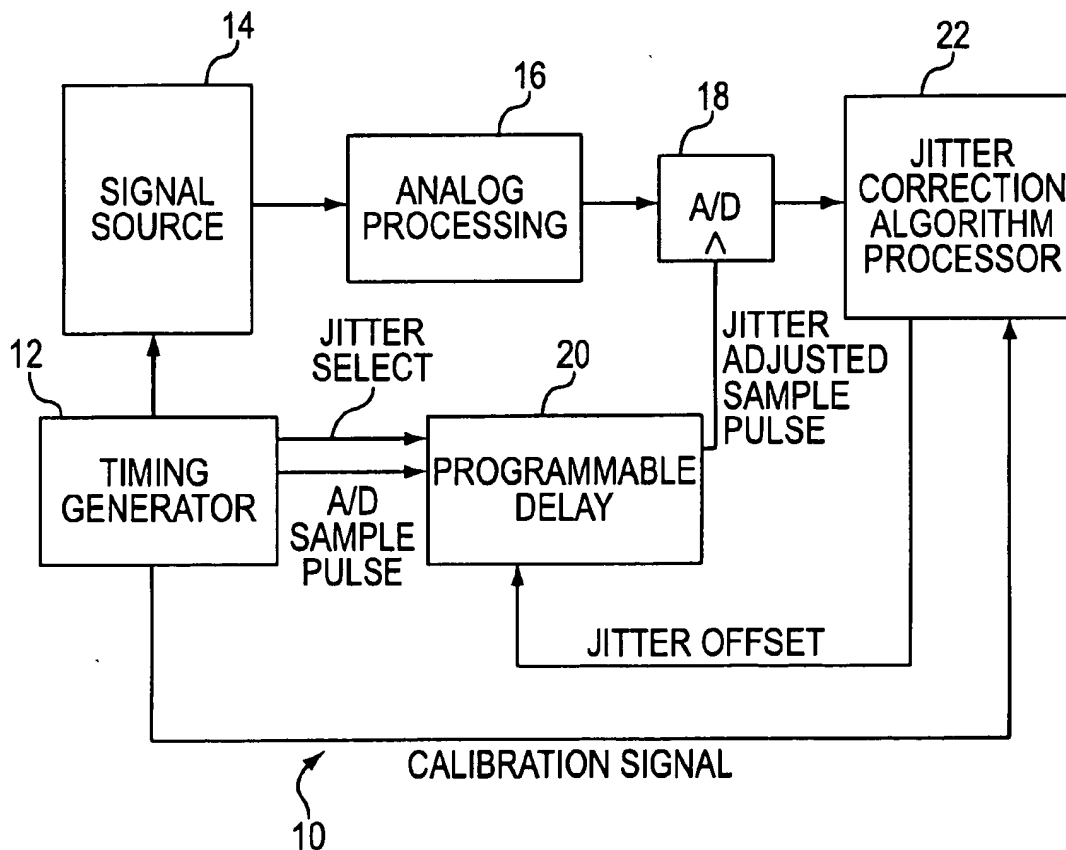
**Related U.S. Application Data**

(60) Provisional application No. 60/229,122, filed on Aug. 31, 2000, and provisional application No. 60/229,054, filed on Aug. 31, 2000.

(51) Int. Cl.<sup>7</sup> ..... **H03M 1/12**

(52) U.S. Cl. .... **341/157; 341/155**

(58) Field of Search ..... 341/155, 143,  
341/144, 118, 119, 120, 121, 122





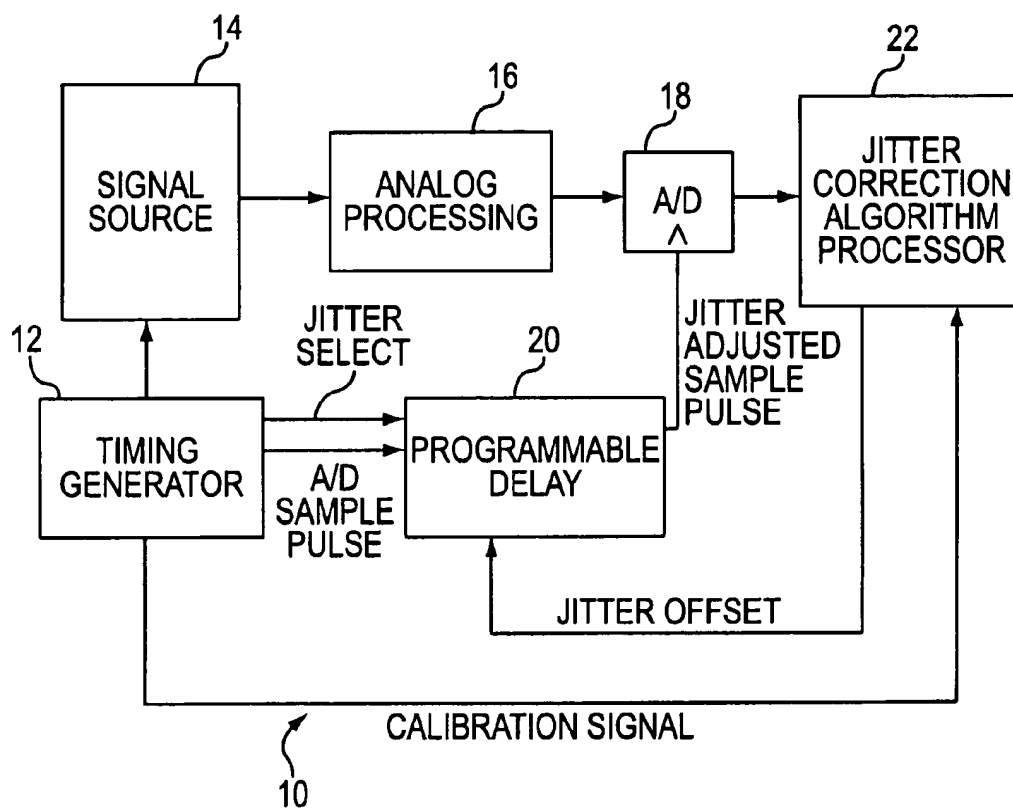


FIG. 1

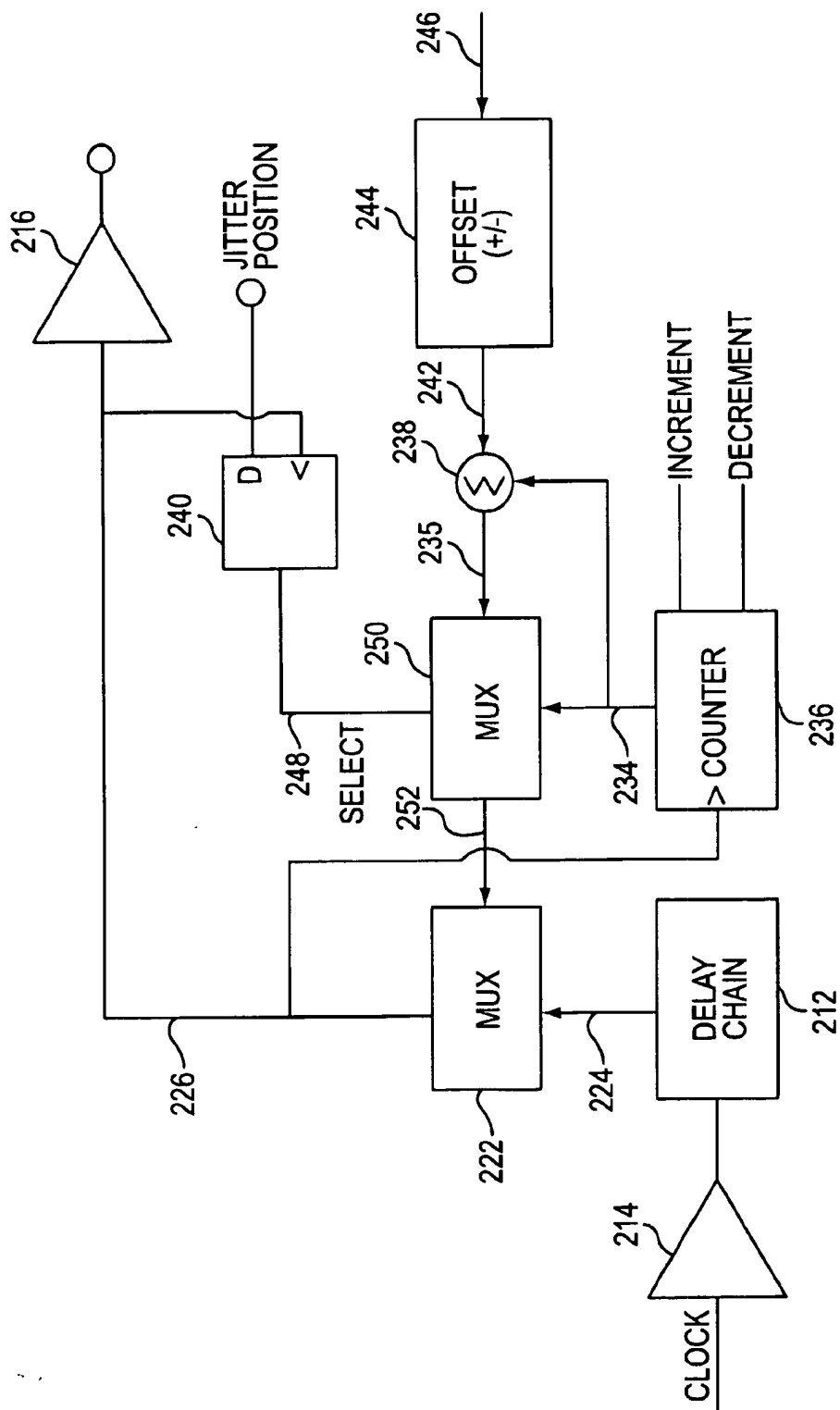


FIG. 2

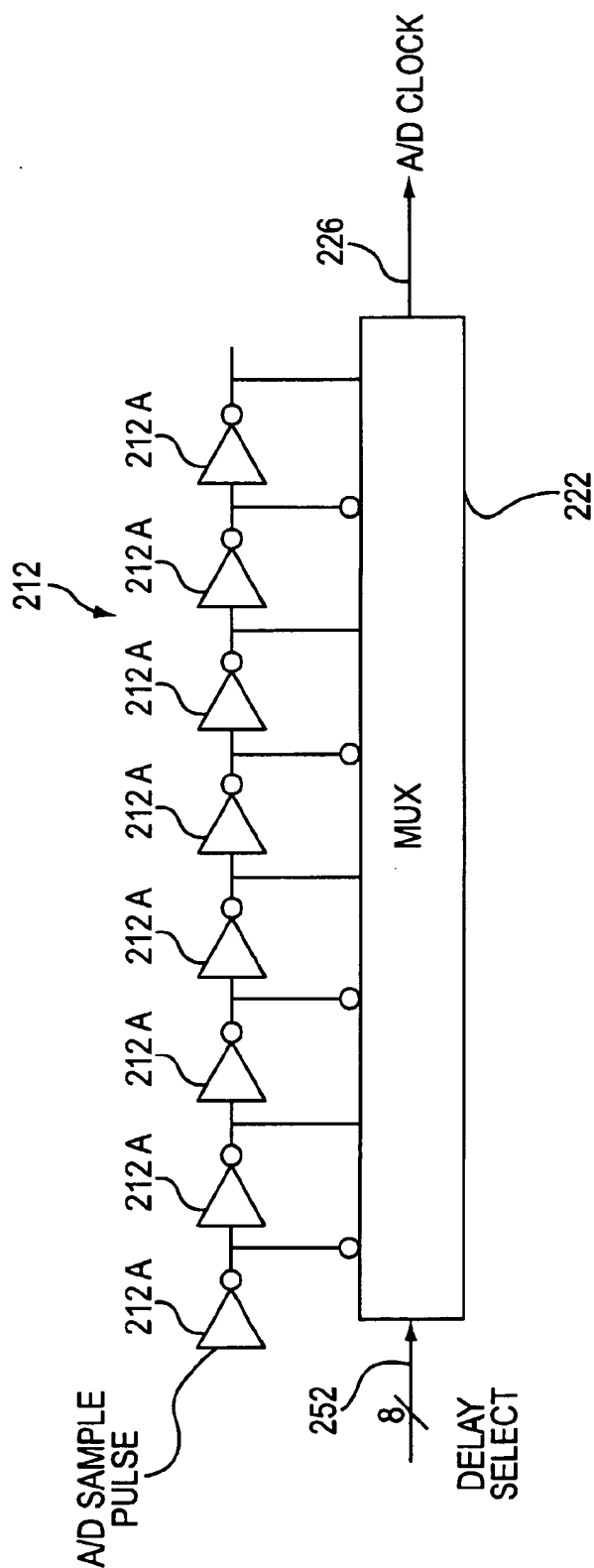


FIG. 3

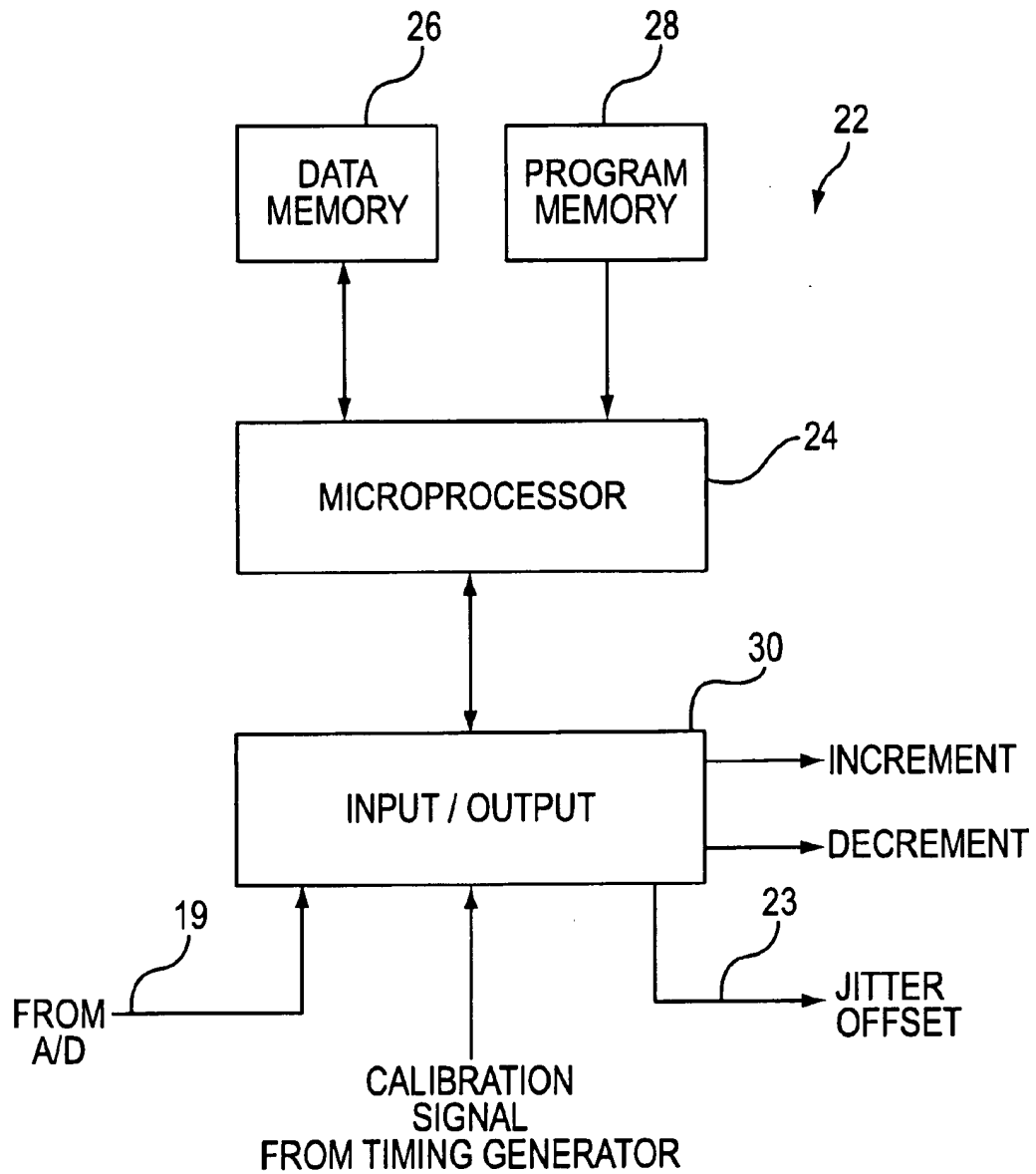


FIG. 4

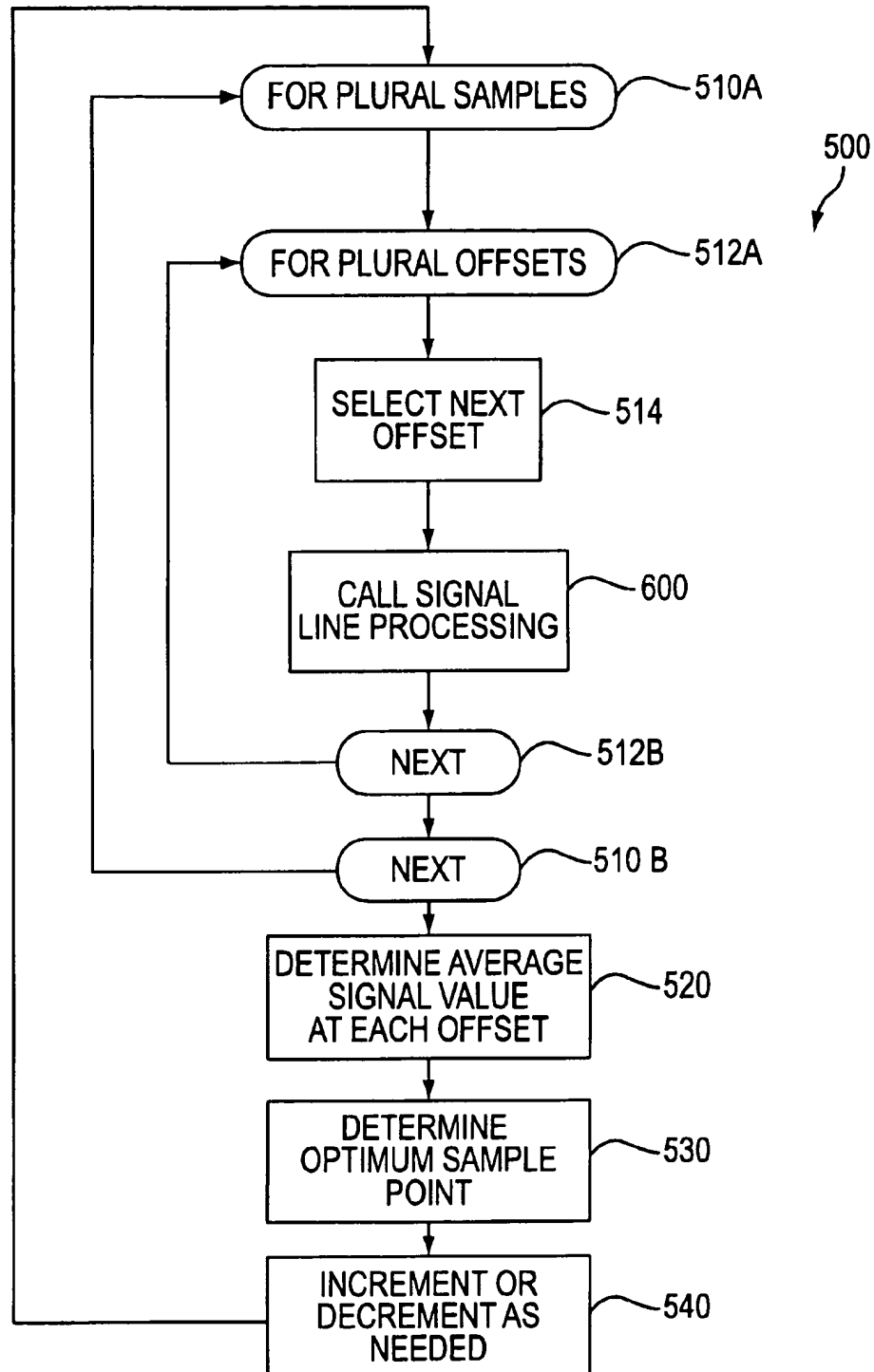


FIG. 5

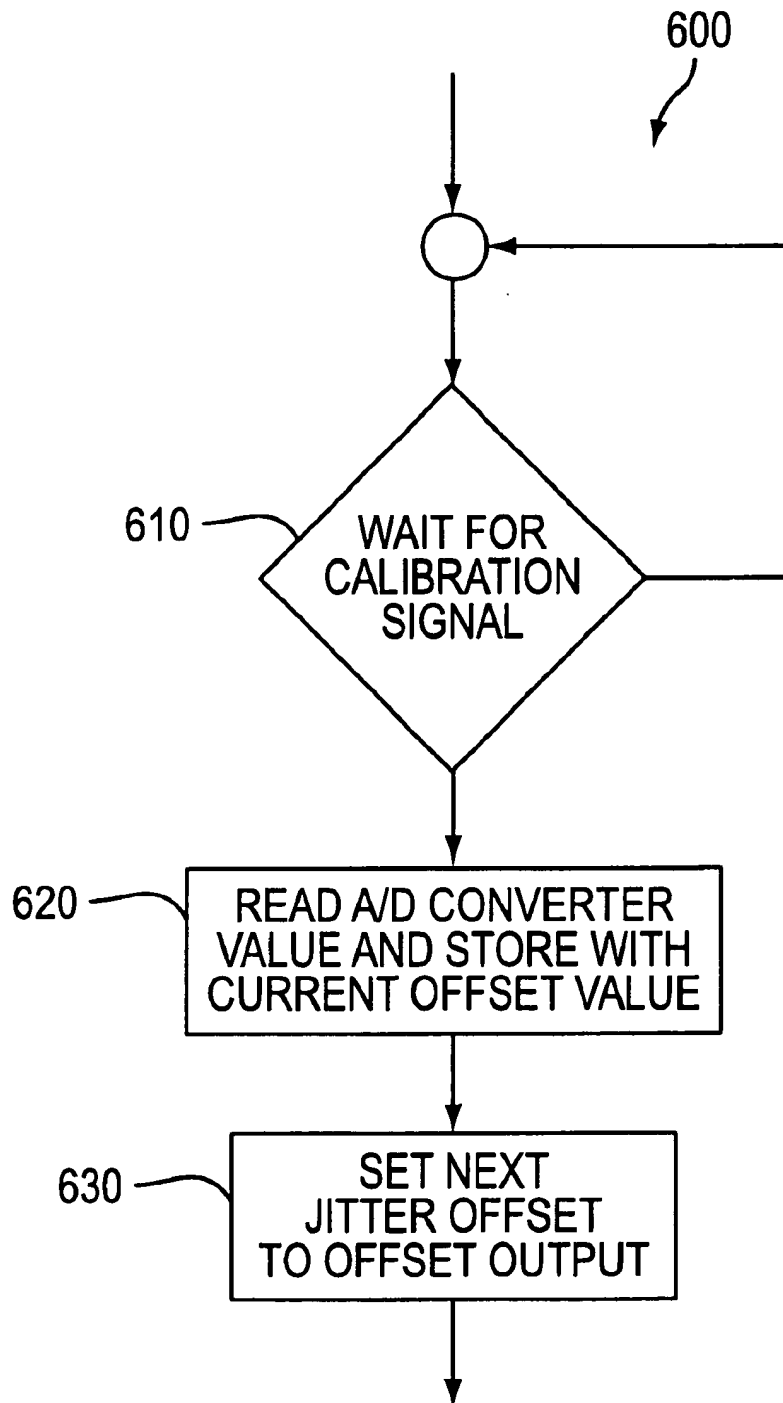


FIG. 6

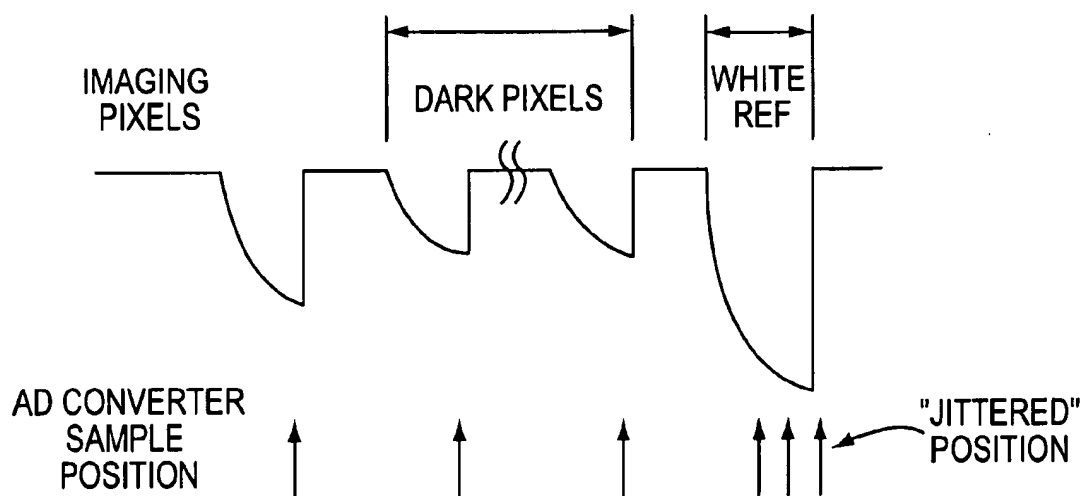


FIG. 7

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## AUTOMATIC A/D CONVERT POSITIONING CIRCUIT AND METHOD

The priority benefits of the Aug. 31, 2000 filing date of provisional application Ser. No. 60/229,122 and of the Aug. 31, 2000 filing date of provisional application Ser. No. 60/229,054 are hereby claimed.

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to positioning the sample time of an analog to digital converter in a periodic waveform.

#### 2. Description of Related Art

It is desired to be able to position the A/D converter pulse in a very narrow window of time and to perform the correct placement over various temperature ranges, supply voltage variations, and component lot to lot variations. In the past, the window of time was set large enough so that any variations in the time placement would not exceed the window width. However, now that there is a greater demand for faster camera sensors and other equipment, this window has shrunk and the old method is no longer adequate. In the past, the time window of the A/D converter position was large enough to accommodate slight variations due to temperature variations, voltage variations and lot to lot variations. The new method is an improvement because it will now be possible to shrink the convert window, and as a result, be able to increase the maximum frequency of operation and provide optimal performance over all operating conditions.

Such variations as clock driver lot to lot variations, voltage and temperature delay variations, analog processing lot to lot variations, timing generation lot to lot variations, and A/D aperture delay lot to lot variations are critical at high speed where timing margin is near zero. These variables are continuously monitored with the present invention and corrected using a digital algorithm and a new delay line capable of "jittering" the sample pulse for one full clock period.

### SUMMARY OF THE INVENTION

It is an object to the present invention to automatically position the sample time of an analog to digital converter.

These and other objects are achieved in a circuit that includes a programmable delay circuit, an A/D circuit triggered by the programmable delay circuit and a jitter correction algorithm processor coupled to insert a standard signal into the A/D circuit and to control the programmable delay circuit.

Alternatively, these objects are achieved with a method that includes steps of measuring a calibration function, correlating the measured calibration circuit with a known function, and determining a jitter control delay value from a result of the step of correlating.

### BRIEF DESCRIPTION OF DRAWINGS

The invention will be described in detail in the following description of preferred embodiments with reference to the following figures wherein:

FIG. 1 is a block diagram of a representative circuit of the invention;

FIG. 2 is a block diagram of the programmable delay circuit of the invention;

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FIG. 3 is a schematic diagram of a delay line and multiplexer of the invention;

FIG. 4 is a block diagram of a jitter correction algorithm processor;

FIG. 5 is a flow chart of a representative algorithm according to the invention;

FIG. 6 is a flow chart of a representative method to measure the calibration function according to the invention; and

FIG. 7 is a graph illustrating the signal into the A/D converter that is processed by the invention based on an imaging sensor chip as a signal source where imaging pixels are preceded by a "white" calibration reference then two dark pixels (the jittered position is illustrated).

### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In FIG. 1, circuit 10 includes timing generator 12 for generating timing and control signals to control signal source 14. Signal source 14 is preferably a CMOS or CCD imaging sensor with associated clock drivers, but could be another type of source such as a communications source such as an "eye" detector. Source 14 generates an analog data signal that includes a test signal incorporated in the signal datastream. The signal datastream, including test signal, is processed through analog processor 16 through to analog to digital converter 18 (A/D converter or ADC). Timing generator 12 also produces an A/D sample pulse that passes through programmable delay circuit 20 to provide a jitter adjusted sample pulse to be used as the sample trigger for A/D converter 18. The digital sampled data from A/D converter 18 is provided to and processed by jitter correction algorithm processor 22. The test signal in the datastream is a calibration signal that is periodically inserted in the signal datastream. For example, in the case of a CCD or CMOS sensor, a pixel data line is read out to include a couple of "dark" pixels, a line of signal pixels, a couple more "dark" pixels and a test pixel, actually a reference white pixel, and the data line is repeated. In the case of communication system, a test signal might be a reference "eye" inserted in the datastream.

Timing generator 12 also provides to jitter correction algorithm processor 22 a calibration signal to indicate when a test signal is present in the datastream sampled by A/D converter 18. In any particular design, the calibration signal may be a pulse in advance of the actual test signal in the datastream. In order to control the programmable delay circuit 20, jitter correction algorithm processor 22 issues a jitter offset signal to the programmable delay circuit 20. Timing generator 12 also provides a jitter select signal to programmable delay circuit 20. The jitter select signal causes programmable delay circuit 20 to jitter the delay through programmable delay circuit 20 (i.e., jitter the jitter adjusted sample pulse) by an amount defined by the jitter offset received from jitter correction algorithm processor 22. However, timing generator 12 controls the timing of the datastream from signal source 14 and the jitter select signal so that the jitter adjusted sample pulse is only jittered when the test signal is present in the datastream and about to be sampled by A/D converter 18. This will be described in further detail with respect to a discussion of programmable delay circuit 20.

Jitter correction algorithm processor 22 collects digital data corresponding to the output of A/D converter 18 when the test signal is being digitally sampled. Typically, 5 to 30 different sample positions, preferably 10 to 20 sample



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positions, spanning a critical time interval, are used to sample the test signal by A/D converter 18. At each sample position, plural samples may be taken to obtain averages. For example, with a CCD or CMOS sensor having 525 lines of pixels (as in an NTSC TV television standard), each frame provides 525 opportunities to measure the test signal. Jitter correction algorithm processor 22 may be structured to collect 35 data samples at each jittered position of 15 sample position spanning the test signal ( $15 \times 35 = 525$ ). For each of the 15 sample positions, the 35 samples taken at the sample position are averaged to determine the mean signal strength at the sample position, and a square root of a variance of the 35 samples around the mean signal strength at the sample position is determined as a measure of the noise. From this, the signal to noise ratio at each jittered sample position can be determined. The mean signal strength at all the 15 sample positions defines a measured test function or calibration function.

The calibration function is correlated with a known reference function to determine the optimum sample point as discussed below. Alternatively, a maximum value of the signal to noise ratio is selected from the plural sample positions (e.g., 15 sample positions in this case).

In FIG. 2, A/D sample pulse from timing generator 12 is provided to an input of input buffer 214 as a clock signal. Input buffer 214 provides the clock pulse to delay chain 212. Delay chain 212 includes plural inverter circuits in a chain (for example, 128 or 256 inverter circuits) generating a multi-tap delay line. Multiplexer 222 is coupled to the plurality of taps generated by delay chain 212 and controlled by shift signal 252 to select a single tap signal 226 that is provided to an input of output buffer 216 that provides the jitter adjusted sample pulse to A/D converter 18.

In FIG. 2, jitter offset signal 242 is an offset to circuit delay signal 234. Jitter offset signal 246 from jitter correction algorithm processor 22 is stored in register 244 (or register 244 might be the output register of processor 22) as signal 242 and added to circuit delay signal 234 in adder 238 to provide jittered signal 235. Tap counter 236 provides circuit delay signal 234 where either signal INCREMENT or signal DECREMENT (from processor 22) increments or decrements counter 236 synchronously with the pulse signal 226. Multiplexer 250 provides shift signal 252 by selecting either circuit delay signal 234 or jittered signal 235 according to a value of select signal 248. Select signal 248 comes either directly from timing generator 12 or, preferably, from D type flip flop 240 (as shown) that is set synchronously by pulse signal 226 where the jitter position input to D type flip flop 240 comes from timing generator 12.

In operation, a clock pulse (e.g., A/D sample pulse from timing generator 12) passes through input buffer 214 and enters delay chain 212. Multiplexer 222 selects single tap 226 from all taps 224 of delay chain 212 based on shift signal 252 used as a selection address. Single tap 226 passes through output buffer 216 to trigger a sample at A/D converter 18 (see FIG. 1). Shift signal 252 is provided by multiplexer 250 by selecting either circuit delay signal 234 or jittered signal 235 according to a value of select signal 248.

Assume for a moment that select signal 248 is set so that multiplexer 250 selects only circuit delay signal 234 to be provided as shift signal 252. In this case, processor 22 is free to increment or decrement counter 236 to adjust the delay between when a clock pulse enters input buffer 214 and exits output buffer 216. The question is, how does processor 22 know whether to increment or decrement?

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To understand this, assume that the circuit of FIG. 2 is used to input the A/D sample pulse from timing generator 12 and to output a pulse timed to strobe A/D converter 18 that samples the sensor's output video data stream. Assume further that the video data stream (a single analog signal) has, in sequence, a couple of dark pixels, a line of data pixels, a couple more dark pixels and then a reference white pixel, and the sequence repeats. Processor 22 is now able to increment or decrement counter 236 based on data received that corresponds to the reference white pixel.

To measure and determine a desired offset, processor 22 loads an offset into offset register 244 that is selected within a range from minus a value to plus the value (e.g. 15 sample positions from -7 to +7 as discussed in the example above): Then, just before the last pixel before the reference white pixel is being read out, the jitter position signal from processor 22 is set to be loaded in D type flip flop 240 when A/D converter sample pulse for the last pixel passes through output buffer 216. This causes multiplexer 250 to provide jittered signal 235 as shift signal 252. Now, when the reference white pixel is converted in A/D converter 18 based on the jittered timing of a strobe from output buffer 216, its sample point will be jittered plus or minus around the count located in counter 236 according to the value in jitter register 244.

Just before the pulse that strobes the reference white pixel passes through output buffer 216, the jitter position signal from processor 22 is reset so that upon the strobe, D flip flop 240 is reset and multiplexer 250 again provides circuit delay signal 234 from counter 236 as shift signal 252. The result of this measurement process is that a single A/D converter sample has been taken of the reference white pixel at a strobe time defined by offset jitter signal 246 for each line from the datastream.

This process is repeated for each video line of the sensor, collecting one calibration sample at a jittered position for each line. After a number of lines, the reference white pixel will have been sampled over a sequence of offset jitter times so as to trace out a complete timeline of the reference white pixel in what is referred to as a calibration function. Processor 22 then correlates this calibration function with a similar known function to determine the optimal time position for A/D converter sampling. Alternatively, processor 22 determines the jitter offset that produces a sample position that exhibits the greatest signal to noise ratio, and then determines the optimal time position for A/D converter sampling based on a maximum signal to noise ratio. Processor 22 then increments or decrements counter 236 to adjust the sampling time of the rest of the video lines following a determination that the optimal sample time has shifted.

This jitter process determines whether or not a convert position is optimal. Typically, only one pixel is used to determine the optimal position of, for example, an A/D converter convert pulse. The increment and decrement signals are provided to control tap counter 236. This tap counter implements a programmable delay that is updated once per frame based on plural samples collected once per line via an algorithm inside processor 22.

In FIG. 3, programmable delay circuit 20 includes plural inverter circuits 212A in a chain (for example, 128 or 256 inverter circuits). The inverter chain is tapped at various points by multiplexer 222 according to shift signal 252 (a delay select signal) provided to the multiplexer. The A/D sample pulse from timing generator 12 is provided into the input of the inverter chain, and the output of the multiplexer 222 is an A/D clock that carries the jitter adjusted sample pulse.

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In FIG. 4, jitter correction algorithm processor 22 includes a microprocessor 24, data memory 26, program memory 28 and input/output logic 30, or other suitable processing arrangement (e.g., ASIC, FPLA, etc.). Processor 22 receives as inputs the digitized signal 19 from A/D converter 18 and a calibration signal from timing generator 12 that identifies when a reference test signal will be sampled by A/D converter 18. Processor sends as output jitter offset 23 to programmable delay circuit 20 to jitter the sample time of each reference test signal embedded in the datastream. When sufficient jittered data has been sampled to determine that an offset is needed for all data being sampled, increment and decrement commands to the tap counter are issued by processor 22. In processor 22, the jitter correction algorithm will shift the position of the A/D converter clock (using increment and decrement), in time, based on a generalized performance (jitter correction) algorithm. Utilization of a pre-specified "white" pixel is employed in the jitter correction algorithm, or in cases where the "white" pixel is not available, any standard imaging pixel can be utilized. The algorithm functions in a manner to optimize (maximize) the response due to the aforementioned "white" pixel and/or minimize noise. The algorithm works by moving the A/D converter sample clock back or ahead in time while monitoring the output response due to the selected reference pixel. The moving back or ahead in time of the A/D converter sample clock is performed by a new programmable delay circuit (FIG. 2). The delay select signal chooses which tap of the inverter chain to direct the A/D converter sample clock signal and hence can control the delay to a resolution determined by the propagation delay through one inverter.

This invention will allow, for example, a camera, to operate reliably at higher frequencies. The programmable delay circuit part of the invention may be used in other applications that require the use of a programmable delay that can be changed "on the fly".

Typically, CMOS buffers will have plus or minus 1 nanosecond drift over the operating temperatures and voltages. This drift, lot to lot, is about 5 nanoseconds according to many data sheets. An A/D converter has about plus or minus 0.5 nanoseconds drift over temperature and voltages of aperture delay. Lot to lot delay may be assumed to be plus or minus 1.5 nanoseconds. Adding up the delays one gets approximately 10 nanoseconds variability, lot to lot, and plus or minus 1.5 nanoseconds over temperature. This assumes stable analog delays. In a sensor chip with correlated double sampling with overdrive, the delay has about a 3 nanosecond window. The programmable delay line approach should compensate for variations in a range from minus 1.5 nanoseconds to plus 14.5 nanoseconds (a 16 nanoseconds range). The resolution should be at least 5 steps in a 3 nanosecond window. This translates to 0.6 nanoseconds per step. Preferably 10 steps would be available in a 3 nanosecond window, or 0.3 nanoseconds. Therefore, to achieve a variable delay in a range from minus 1.5 nanoseconds to 14.5 nanoseconds (a 16 nanosecond range), 32 steps might be required at 0.5 nanoseconds per step.

Sometimes inductance-capacitance cells may be used for delay lines; however, phase jitter due to unrelated switching may result in and create undesirable effects. Furthermore such delay lines are not consistent, lot to lot, or part to part, or over temperature.

In FIG. 5, a flow chart of the jitter correction algorithm includes loop controls 510A, 510B, 512A and 512B. Loop controls 510A and 510B merely loop enough times to obtain sufficient calibration samples to perform good averaging. In

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the NTSC example discussed above, 35 loops are performed. Loop controls 512A and 512B alter the jitter offset for the measurements. In the NTSC example discussed above, 15 loops are performed. At the beginning of each loop, the next offset (not the current one being measured) is selected at step 514, and the algorithm calls signal line processing 600, a step discussed below with respect to FIG. 6.

After all loops are performed by loop controls 510A, 510B, 512A and 512B, the stored data is processed in step 520. This might mean an end of a frame of signal lines as in the NTSC example discussed above, or it might mean at the end of a predetermined number of signal lines whether or not organized in frames. In step 520, the data is set into bins corresponding to each jittered offset. All test signal values within a bin (i.e., a single offset value) are averaged. FIG. 7 depicts a representative graph of a signal datastream with a white reference test signal at the end of the datastream. In the NTSC example discussed above, the 15 averaged sample values will trace out a curve that is a discrete time sampled version of the white reference test signal.

In step 530, a new optimum sample point is determined. One way to do this is to determine the signal to noise ratio of measured data at each sample point. The signal is the average signal value determined by step 520. A noise metric at each jittered offset is determined by calculating, for example, the square root of a variance about the mean of all test signal values within a bin (i.e., at a single offset value). Then, the ratio can be determined. The greatest signal to noise value indicates the optimum signal point. Presumably, the noise is somewhat consistent at each jittered sample point, thus, the signal noise ratio will tend to peak where the averaged signal is greatest. The optimal sample point is taken as the offset where the signal to noise ratio is greatest.

Alternatively, the optimal sample point may be determined by correlating in time the measured calibration function (i.e., the averaged measurements at each jitter sample position) with a known calibration function and choosing the expected optimal point of the known function based on an offset of the measured calibration function from a known calibration function.

In step 540, the value of tap counter 236 (FIG. 2) is incremented or decremented to adjust the count value to perform optimal sampling at all points in the datastream, not just the test signal. For example, if jittered offsets are tested between -7 and +7 tap positions relative to the value of tap counter 236, where the 0 tap position is taken to be the current value of the tap counter, and if the optimal jittered offset is calculated to be +1, then the tap counter will be incremented. Then, during the next frame of data (or plurality of lines of data, if not organized in frames), the optimal jittered offset will be reduced to a 0 tap position again unless further delay line jitter occurs.

In FIG. 6, signal line processing 600 includes the steps of step 610 of waiting for the calibration signal from the timing generator, step 620 of reading the A/D converter value and storing it with the current offset value, and step 630 of setting up the next offset value by outputting the next offset value to programmable delay circuit 20 to be ready for the next time that timing generator 12 strobes programmable delay circuit 20 with a jitter select.

In FIG. 7, there is illustrated a timeline of a signal source coming from a pixel line of an imaging sensor. A white reference pixel is included in the datastream. The jitter position is shown with the white reference pixel to be varied over a limited range where the white reference pixel has its

maximum value. Once this variation is sampled and correlated according to the jitter correction algorithm, the correct value for the jitter delay is set for the next line.

Having described preferred embodiments of a novel A/D convert positioning circuit and method (which are intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments of the invention disclosed which are within the scope and spirit of the invention as defined by the appended claims.

Having thus described the invention with the details and particularity required by the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.

What is claimed is:

1. A circuit comprising:

a programmable delay circuit to provide a strobe;  
an A/D circuit triggered by the strobe; and  
a jitter correction algorithm processor coupled to control the programmable delay circuit to jitter in time the strobe when a test sample is input into the A/D circuit.

2. A circuit comprising:

a programmable delay circuit to provide a sequence of delayed pulses;  
an A/D circuit to convert a sequence of values into digital values sampled at times defined by the sequence of delayed pulses; and  
a jitter correction circuit to adjust the programmable delay circuit based on a sequence of digital values from the A/D circuit sampled at times defined by the sequence of delayed pulses.

3. The circuit of claim 2, further comprising a timing generator, wherein timing generator provides the jitter correction circuit with a calibration signal to define when a test signal will be input into the A/D converter.

4. The circuit of claim 3, wherein the jitter correction circuit includes:

an input to receive the sequence of digital values and the calibration signal;  
an output to provide a jitter offset;  
a processor coupled to the input and to the output; and  
a memory coupled to the processor.

5. The circuit of claim 4, wherein the jitter correction circuit includes a line processing module stored in the memory to control the processor, wherein the line processing module includes:

a sub-module to wait for receipt of the calibration signal;  
a sub-module to read a value from the A/D converter and store the value and a current offset in a data memory; and  
a sub-module to provide a next jitter value to the programmable delay circuit.

6. The circuit of claim 5, wherein the jitter correction circuit further includes:

a module to select a next jitter offset; and  
a module to iteratively repeat the module to select a next jitter offset and the sub-modules of the line processing module.

7. The circuit of claim 6, wherein the jitter correction circuit further includes:

a module to determine a calibration function;  
a module to determine an optimum sample point from the calibration function; and

a module to adjust the programmable delay circuit based on the optimum sample point.

8. The circuit of claim 2, wherein the jitter correction circuit includes:

an input to receive the sequence of digital values;  
an output to provide the jitter control delay value and a multiplexer control signal, the multiplex control value being coupled to the multiplexer;  
a processor coupled to the input and to the output; and  
a memory coupled to the processor.

9. The circuit of claim 8, wherein the memory has stored therein modules for controlling the processor, the modules including:

a first module to control the processor to measure a test signal transmitted as part of a datastream at a plurality of offsets from a nominal sample time;  
a second module to control the processor to determine an average measured value at each offset; and  
a third module to control the processor to determine an optimal offset from the nominal sample time.

10. The medium of claim 9, further comprising a fourth module to control the processor to adjust a programmable delay circuit according to the optimal offset.

11. The medium of claim 9, wherein the first module includes:

a first sub-module to control the processor to select an offset for a next test sample;  
a second sub-module to control the processor to wait for a calibration signal from a timing generator;  
a third sub-module to control the processor to measure a digital value of the test signal at a current offset when the calibration signal is received; and  
a fourth sub-module to control the processor to set the selected next offset in a programmable delay circuit.

12. The circuit of claim 2, wherein the circuit is a circuit integrated on a single chip.

13. The circuit of claim 2, wherein the circuit is part of a sensor integrated on a single chip.

14. A circuit comprising:

a programmable delay circuit;  
an A/D circuit triggered by the programmable delay circuit; and  
a jitter correction algorithm processor coupled to examine a test signal transmitted as part of a data stream and to control the programmable delay circuit.

15. A method comprising steps of:

measuring a test signal transmitted as part of a datastream at a plurality of offsets from a nominal sample time;  
determining an average measured value at each offset; and  
determining an optimal offset from the nominal sample time.

16. The method of claim 15, further comprising a step of adjusting a programmable delay circuit according to the optimal offset.

17. The method of claim 15, wherein the step of measuring a test signal includes steps of:

selecting an offset for a next test sample;  
waiting for a calibration signal from a timing generator;  
measuring a digital value of the test signal at a current offset when the calibration signal is received; and  
setting the selected next offset in a programmable delay circuit.

18. A computer readable medium having stored therein modules for controlling a processor, the modules including:

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a first module to control the processor to measure a test signal transmitted as part of a datastream at a plurality of offsets from a nominal sample time;

a second module to control the processor to determine an average measured value at each offset; and

a third module to control the processor to determine an optimal offset from the nominal sample time.

19. The medium of claim 18, further comprising a fourth module to control the processor to adjust a programmable delay circuit according to the optimal offset.

20. The medium of claim 18, wherein the first module includes:

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a first sub-module to control the processor to select an offset for a next test sample;

a second sub-module to control the processor to wait for a calibration signal from a timing generator;

a third sub-module to control the processor to measure a digital value of the test signal at a current offset when the calibration signal is received; and

a fourth sub-module to control the processor to set the selected next offset in a programmable delay circuit.

\* \* \* \* \*



US006430715B1

(12) **United States Patent**  
**Myers et al.**

(10) Patent No.: **US 6,430,715 B1**  
(45) Date of Patent: **Aug. 6, 2002**

(54) **PROTOCOL AND BIT RATE INDEPENDENT TEST SYSTEM**

(75) Inventors: **Kenneth T. Myers; Douglas J. Gardner, both of Palm Harbor, FL (US)**

(73) Assignee: **Digital Lightwave, Inc.**

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(21) Appl. No.: **09/533,582**

(22) Filed: **Mar. 23, 2000**

**Related U.S. Application Data**

(60) Provisional application No. 60/154,686, filed on Sep. 17, 1999.

(51) Int. Cl.<sup>7</sup> ..... **G06F 11/00; G01R 31/28**

(52) U.S. Cl. .... **714/704; 714/712**

(58) Field of Search ..... **714/704, 708, 714/709; 375/321, 224; 359/110, 180**

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*Primary Examiner*—Albert Decady

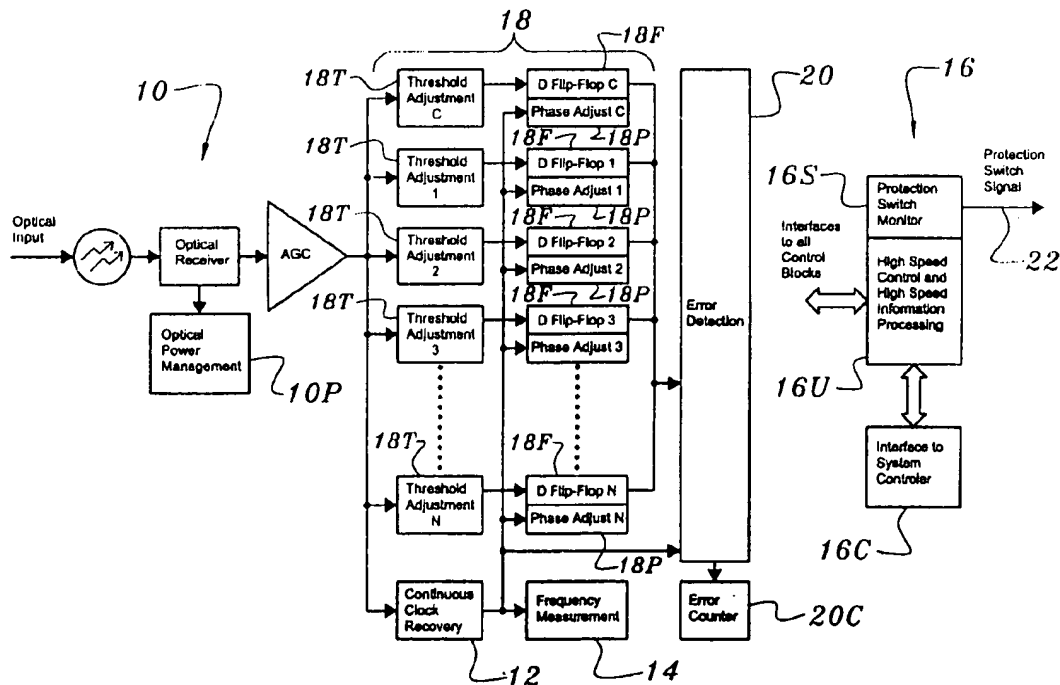
*Assistant Examiner*—Joseph D. Torres

(74) *Attorney, Agent, or Firm*—Holland & Knight LLP

(57) **ABSTRACT**

A protocol and bit rate independent test system for detecting bit errors on a digital communications channel regardless of format or rate, comprising a receiver for receiving an input, a clock recovery unit, a threshold sampling circuit for providing at least two threshold detectors for respective two sampling points including at least one static sampling point positioned proximate to the center of an eye pattern and at least one dynamic sampling point, the output of which are sampled by the recovered clock and if the signal passes between the thresholds, an error signal is generated and counted.

**28 Claims, 5 Drawing Sheets**



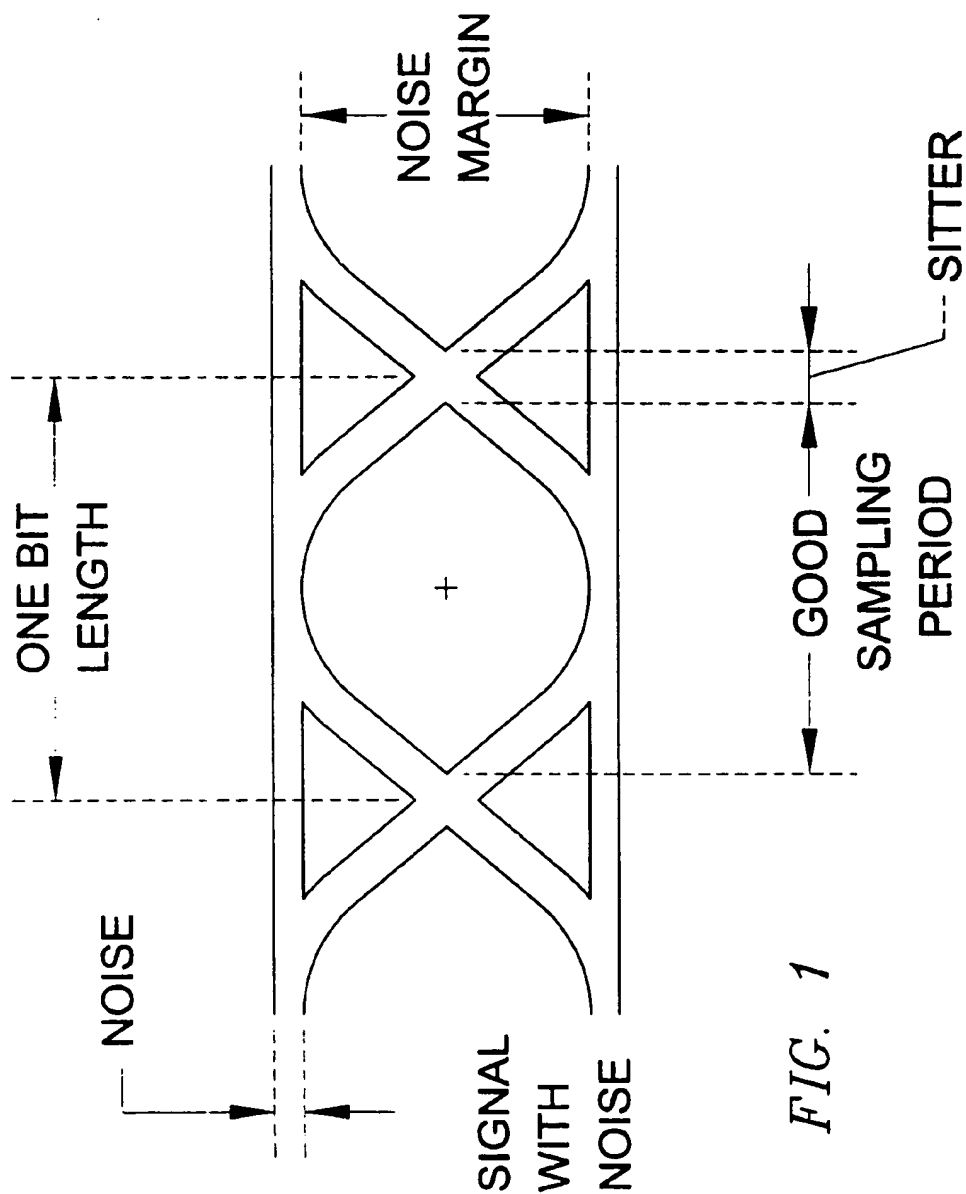


FIG. 1

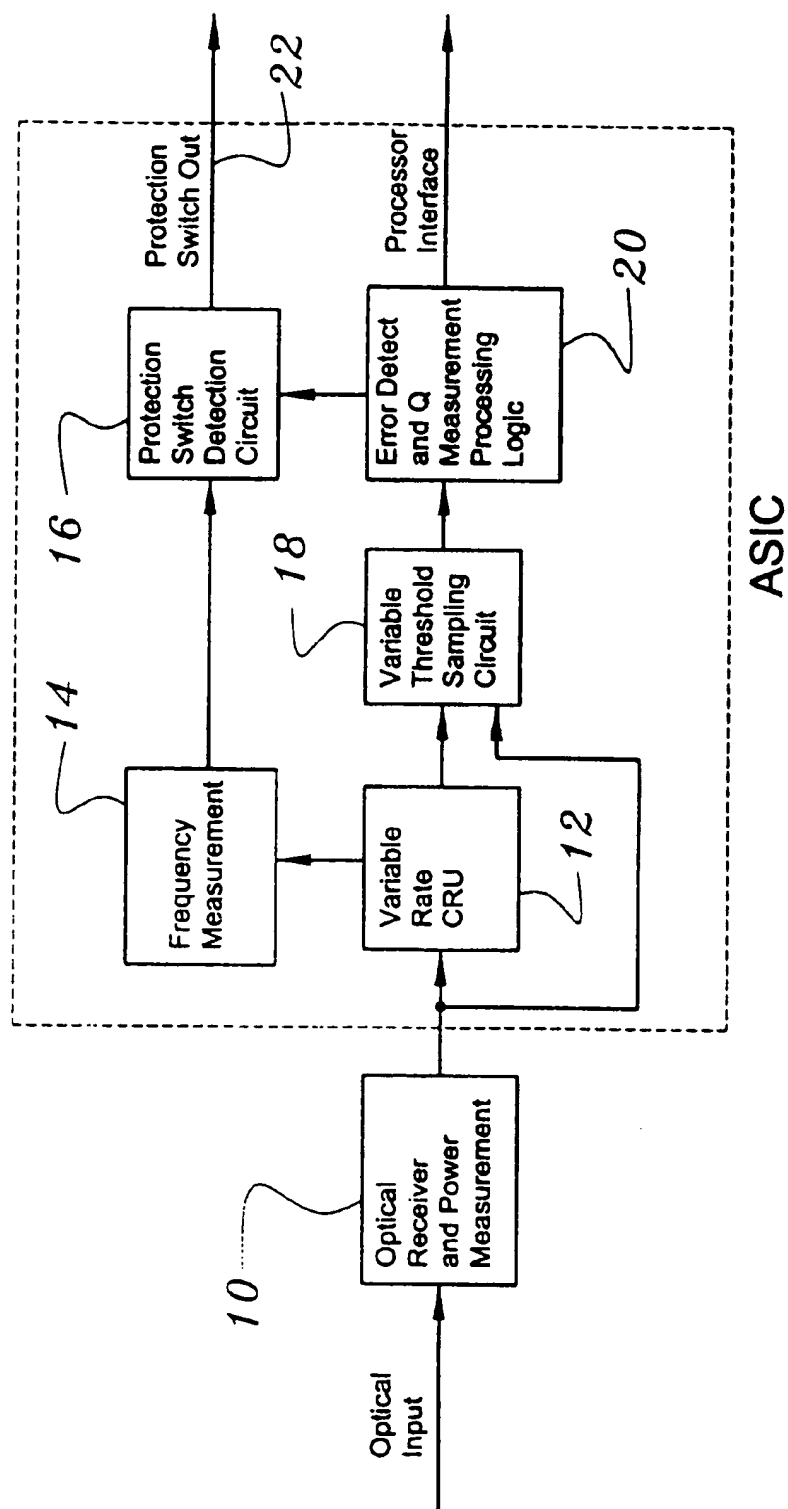
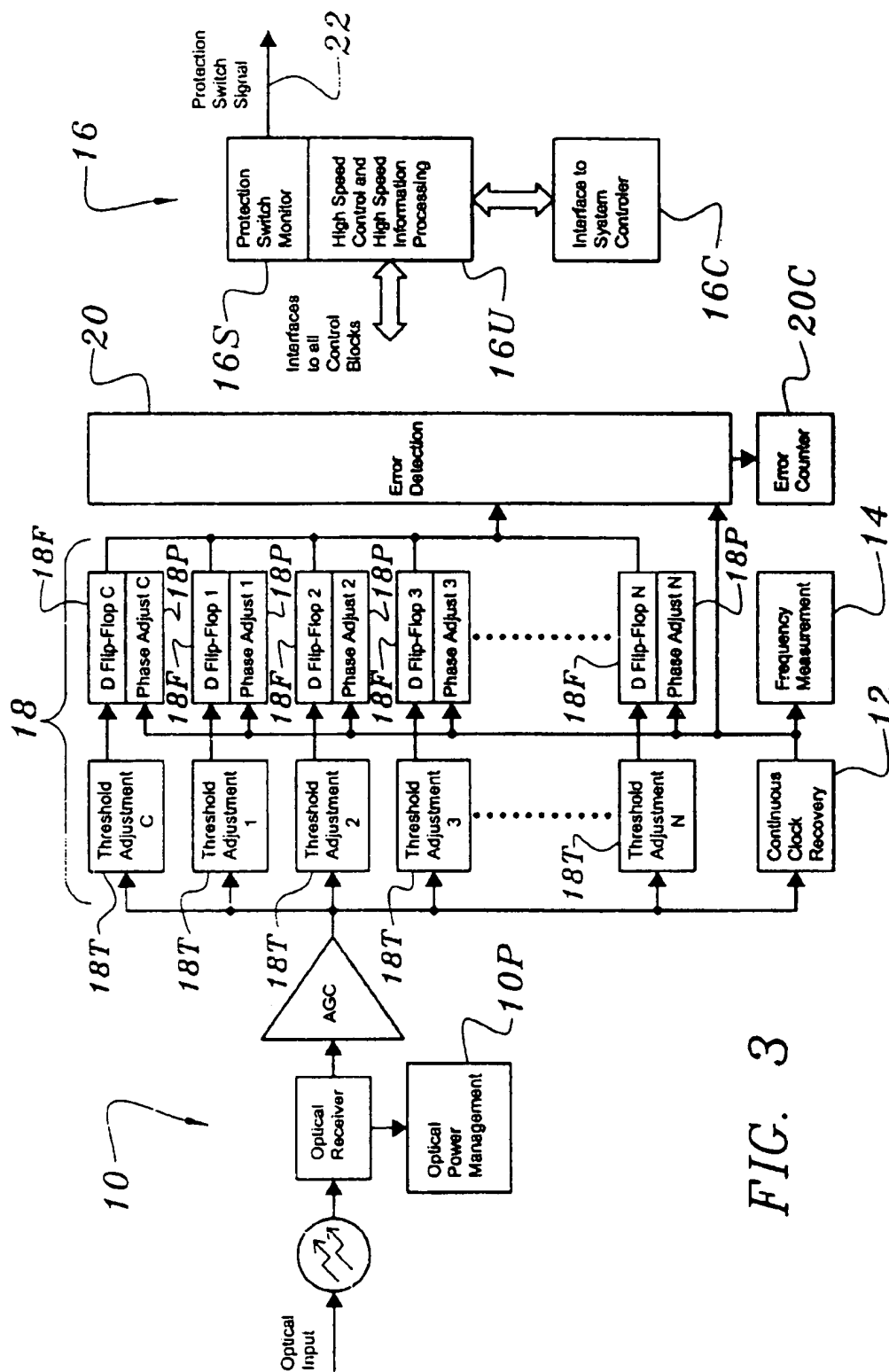


FIG. 2





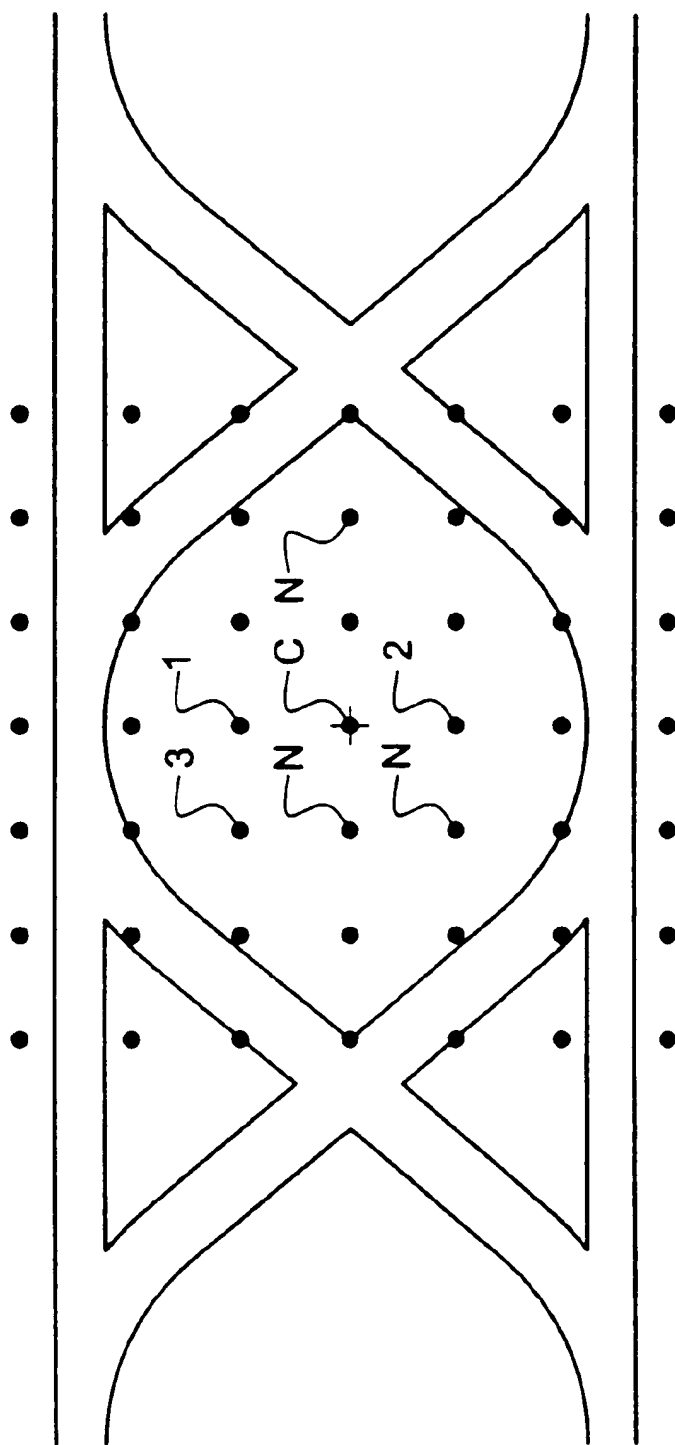


FIG. 4

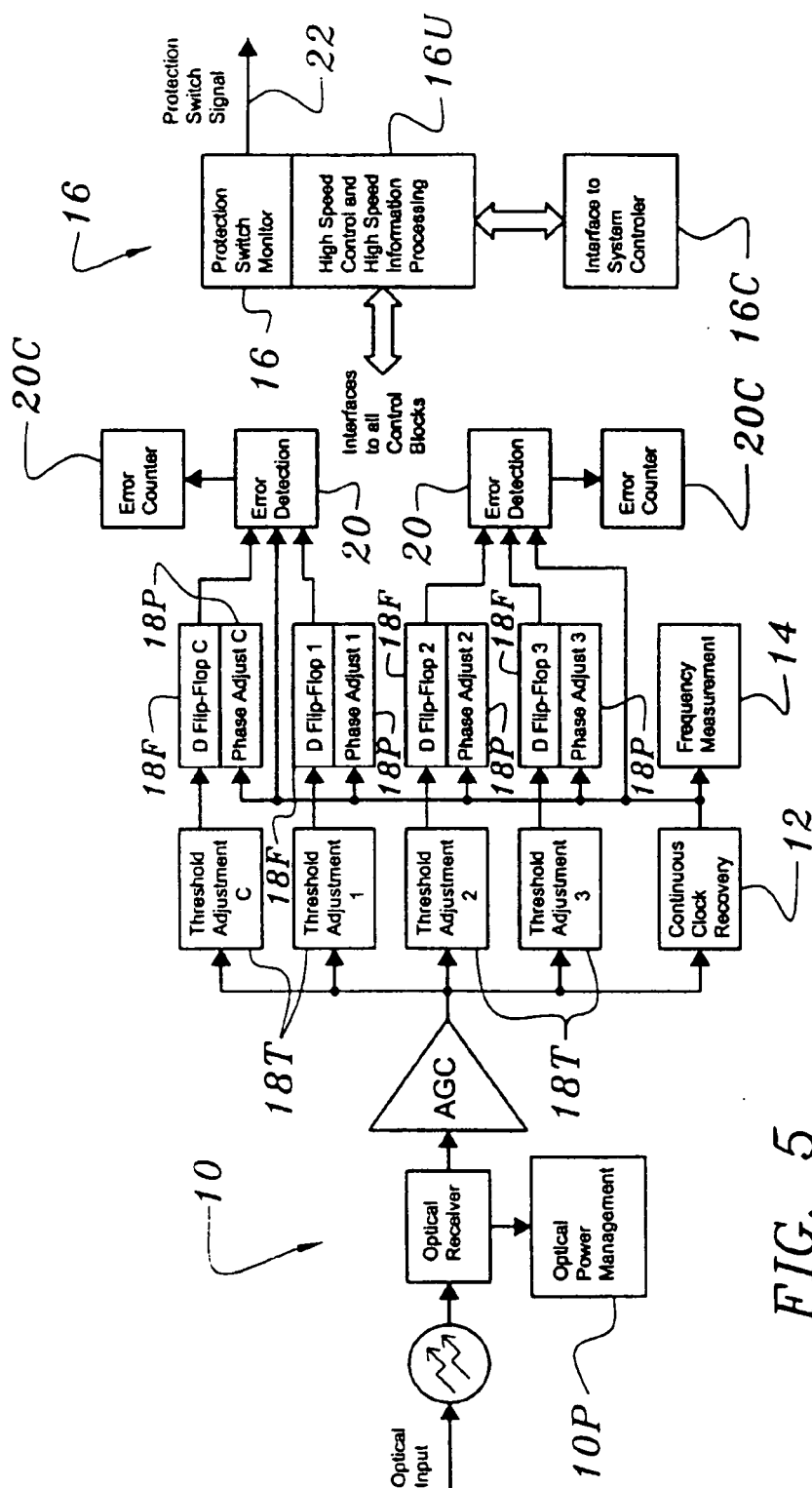


FIG. 5

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## PROTOCOL AND BIT RATE INDEPENDENT TEST SYSTEM

### CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a utility application based upon and claiming priority of provisional application No. 60/154,686, filed Sep. 17, 1999. The disclosure of the provisional application is incorporated herein in its entirety by reference.

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

This invention relates to a protocol and bit rate independent test system for digital communication systems. More particularly, this invention relates to systems that are able to detect bit errors on a digital communications channel regardless of format or rate.

#### 2. Description of the Background Art

In digital communication systems, particularly dense wavelength division multiplexed (DWDM) optical systems, multiple signal formats may exist on the same communications link at different wavelengths. It is useful to be able to extract a signal and determine its health. Hence, there is a need to have a protocol independent and bit rate independent test capability that can (1) detect a single defective bit, (2) monitor the traffic error rate and (3) provide a protection switch signal within milliseconds of exceeding the error threshold condition, and to embed such a test head on every wavelength of the communications system, such as a DWDM system, so as to support such systems where the traffic on different wavelength channels are different protocols and different bit rates. The channels will contain unknown protocols as purchased by the customers. In such a scenario, the customer can buy a wavelength of light and the service carrier does not control the rate or protocol of the traffic. This creates a difficult testing condition since the service provider needs a way to verify error free transmission, provide protection switching and location of the fault condition. The service provider therefore needs a test capability that is bit rate and protocol independent.

Heretofore it has been known that the performance of a communications link, such as a fiber optic link, known as Q factor measurement, is reflected by interpreting the eye pattern of the waveforms of a series of pulses. A typical eye pattern is depicted in FIG. 1. The optimal time for sampling the data signals and the optimal level (the threshold level) at which to distinguish between zeros and ones is the center of the eye. Further, it is known that the height of the central eye opening determines noise margin in receiver output, the width of the signal band at the corner of the eye depicts the jitter or variation in pulse timing in the system, the thickness of the signal line at top and bottom of the eye is proportional to noise and distortion in the receiver output, and transitions between top and bottom of the eye pattern show the rise and fall times of the signal that can be measured on the eye pattern. More complete descriptions of eye measurements (and of receivers and other components) can be found in the following references, the disclosures of each of which are incorporated by reference herein: Joseph C. Palais, *Third Edition Fiber Optic Communications*, Prentice Hall, Englewood Cliffs, N.J., 1992; John B. Anderson, *Digital Transmission Engineering*, IEEE Press, Piscataway, N.J., 1999; Stephen B. Alexander *Optical Communication Receiver Design*, SPIE Optical Engineering Press, Bellingham, Wash., 1997; Govind P. Agrawal *Fiber-Optic Communication Systems*, John Wiley & Sons, Inc, New York N.Y., 1997;

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Kaminow and Koch, *Optical Fiber Telecommunication IIIA*, Academic Press Limited, 1997; and Anderson and Lyle, *Technique for Evaluating System Performance Using Q in Numerical Simulations Exhibiting Intersymbol Interference*, *Electronics Letters*, Vol. 30, No. 1, Jan. 6, 1994. Unfortunately, Q measurements does not provide a real-time measurement or a single-bit error detection capability.

An object of this invention is to provide a bit rate and protocol independent test apparatus and method that can be embedded on every wavelength of a communications system such as a DWDM system.

Another object of this invention is to provide a bit rate and protocol independent capability that can (1) detect a single defective bit, (2) monitor the traffic error rate and (3) provide a protection switch signal within milliseconds of exceeding the error threshold condition of the communications system.

Another object of this invention is to provide an apparatus and method for conducting eye measurements to determine the Q factor.

The foregoing has outlined some of the pertinent objects of the invention. These objects should be construed to be merely illustrative of some of the more prominent features and applications of the intended invention. Many other beneficial results can be attained by applying the disclosed invention in a different manner or modifying the invention within the scope of the disclosure. Accordingly, other objects and a fuller understanding of the invention may be had by referring to the summary of the invention and the detailed description of the preferred embodiment in addition to the scope of the invention defined by the claims taken in conjunction with the accompanying drawings.

### SUMMARY OF THE INVENTION

For the purpose of summarizing this invention, this invention preferably comprises a discrete implementation or custom Application Specific Integrated Circuit (ASIC) including the major components of a receiver, variable rate CRU (Clock Recovery Unit), and a very high speed threshold sampling module for various static or dynamic sampling points positioned in an array (two-dimensional or linear) that is able to instantaneously determine the shape of the eye of a digital communication system, and very high speed logic to process the data. This basic system meets the requirement and is the basis for a universal test set. In addition to bit error detection, it measures the frequency of the signal. Further enhancements includes creating oscilloscope eye diagrams and bit capture and post processing to identify the signal protocol by post processing. The preferred embodiment of the invention has particular application in optical communications systems, such as DWDM optical systems, employing an optical receiver; however, the invention may be incorporated into various other types of digital communication systems employing various other types of receivers without departing from the spirit and scope of this invention.

The foregoing has outlined rather broadly the more pertinent and important features of the present invention in order that the detailed description of the invention that follows may be better understood so that the present contribution to the art can be more fully appreciated. Additional features of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such

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equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

### BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature and objects of the invention, reference should be had to the following detailed description taken in connection with the accompanying drawing in which:

FIG. 1 is an exemplary eye diagram illustrating the various parameters thereof;

FIG. 2 is an overview block diagram of the bit rate and protocol independent test system invention;

FIG. 3 is a high-block diagram of FIG. 2,

FIG. 4 is an exemplary eye diagram incorporating the invention; and

FIG. 5 is the anticipated initial implementation of FIG. 3.

Similar reference characters refer to similar parts throughout the several views of the drawings.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 2, the preferred apparatus of the invention comprises an optical receiver 10 that is preferably either PIN photodiode or avalanche photodiode (APD) based, with the former providing the lower cost. The invention also comprises a variable rate Clock Recovery Unit (CRU) 12 that is preferably phase locked loop (PLL) based to provide the desired flexibility. Frequency measurement 14 of the invention preferably comprises a high speed prescaler which drives a counter and provides a timebase to a protection switch detection circuit 16. A processor (not shown) is provided to measure the length of the divided down frequency to determine the line rate.

As described below in greater detail, the variable threshold sampling circuit 18 provides a plurality of threshold detectors. The output of these threshold detectors is sampled by the recovered clock. The thresholds are set as a percentage of peak eye amplitude and may be programmable. A minimum of two threshold detectors would be required to examine every bit. One threshold would be set in the upper area of the eye (i.e., 80% of peak) and the other set in the lower area of the eye (i.e., 20%). If the signal passes between the thresholds, it is considered an error. These are counted and may be read by a processor from the Error Detect and Q Measurement Processing Logic 20. Additional threshold sampling circuits with spread thresholds may be employed to provide further resolution and grading of each bit.

The protection switch detection circuit 16 compares the counted errors in a given timebase period with a programmable threshold. If exceeded, the protection switch output 22 goes active. This allows fast response to protection switch events with minimal software delays.

Referring now to FIG. 3, a more detailed description of the invention is presented as follows. The invention has an optical fiber input in which the incoming optical signal is fed to the optical receiver 10. The incoming optical power is measured by the power measurement block 10P. The receiver's output feeds the AGC input. The output of the AGC feeds multiple threshold adjustment blocks 18T (C and 1 through N) and the clock recovery unit 12. The clock recovery unit's clock is fed to multiple phase adjustment units 18P (C and 1 through N) that respectively control the clock feeding of multiple D Flip-Flops 18F (C and 1 through N) corresponding to the center data point C of the eye (see FIG. 4) and a plurality of arrayed data points (1 through N)

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positioned in an array about the other areas of the eye. The clock recovery unit also feeds the frequency measurement unit 14. The D Flip-Flops 18F are fed into an error detection circuit 20. The error detection circuit 20 feeds the error counter 20C. A high-speed control unit 16 controls all the threshold and phase adjustments. A high-speed information processing unit 16U processes all the incoming data. The protection switch unit 16S processes all the needed information and provides the protection switch signal 22. The interface unit provides an interface to the system controller 16C.

The anticipated first implementation of the invention is disclosed in FIG. 5 that employs the CRU produced by Vitesse Semiconductor Corp. as disclosed in the article McCormack, *Intelligent Data Recovery, Communication Systems Design*, December, 1999, the disclosure of which is incorporated by reference herein, wherein the D Flip-Flops 18F and phase adjustment units 18P are "paired" and in which an error detection 20 and counter 20C is provided for each pair.

The theory of operation for each of the components is described as follows. The input channel is the analog path that converts the optical signal into a gain adjusted analog electrical signal. This channel includes the Clock Recovery Unit (CRU) which will extract the clock from the incoming data. The optical receiver preferably comprises a PIN receiver followed by an AGC into a variable rate Clock Recovery Unit (CRU). A PIN receiver and AGC is selected to provide a more linear analog channel. The CRU is flexible and provides continuous coverage from approximately 45 Mbit/sec to 2.7 Gbit/sec. Frequency measurement consists of a high speed pre-scaler that drives a counter. The frequency will be measured against a high quality clock source to derive the incoming frequency and also provide a timebase to the protection switch circuit.

The sampling block consists of a multiplicity of D Flip-Flops, such as in the anticipated first implementation, paired D Flip-Flops. There are separate controls of decision threshold and phase of the sampling clock. With control of the threshold and phase, the entire eye can be sampled or scanned across an array as shown in FIG. 4 (the number and positioning of the data points to be optimally determined). The following algorithm is provided as an example. The 1<sup>st</sup> step is to find the optimum sampling position of the eye, typically the center C. After finding the optimum sampling position, one of the D Flip-Flops can be positioned at this location, hence the labeling "C". The other D Flip-Flop can now be used to scan around the eye to determine the margins, shape, and quality of the eye. The outputs of this sampling pair are fed to an error detection circuit that can determine bit value decision differences (decision errors) on a bit by bit real time basis.

Refer now to FIG. 4 for the example eye diagram used for the following description. Sampling point C indicates the center of the eye and point 1 indicates the point of one of the D Flip-Flop pairs. The sample point of this pair C and 1 (as well as the other individual points) can be moved around the eye independently. For example, in FIG. 5, with point C being the center of the eye, point 1 can be moved around to obtain information from the eye or left static to provide real time error information. As point 1 moves into this boundary of the eye, decision errors will start to occur. Combined with other points that may be dynamically moved around or made to remain static, many other decision errors will start to occur. By statistically processing the decision errors, eye profiling and Q measurements can be made. By fixing the relative position of the points, algorithms can be developed

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that will allow for accurate monitoring of the traffic BER. Importantly, the flexibility of the apparatus and method of the invention allows adaptation to the particular implementation with its inherent characteristics (i.e., satellite or microwave).

The control and processing block controls all the system adjustments and access to all the data. This block provides all real time control and data processing. Processing of the controls and error detect circuitry allows for Q measurements and BER analysis. Processing of the errors and clock rate provides a protection switch signal. The programmable nature of the invention allows the service provider to set the parameters to achieve the confidence level required by the customer before generating a protection switch signal. The bit rate affects the time and confidence level obtainable in a given time period. This trade-off is to be optimized with respect to the protection switch time.

Optical Receiver Block should support 1310 nm band and 1550 nm band input optical range and a pin receiver. It is noted that an APD receiver may be required to provide input sensitivity or a PIN receiver may be calibrated to mimic the APD's performance, thus saving the cost of an APD.

Optical Receiver Power Measurement measures the receiver optical power and the optical power from approximately 0 dBm to -35 dBm.

Automatic Gain Control (AGC) Block provides approximately 40 dB of gain range and approximately 20 mV of input sensitivity.

Threshold Adjustment Block provides approximately 64 adjustable threshold steps.

Continuous Clock Recovery Block supports input data rates from approximately 45 Mbit/sec to 2.7 Gbit/sec.

Frequency Measurement Block provides bit rate measurement, a high speed pre-scaler which drives a counter and a high quality clock reference to measure the incoming frequency against.

Phase Adjust Block provides approximately 64 adjustable phase steps.

D Flip-Flip Block provides data sampling and supports threshold adjustments and clock phase adjustments.

Error Detection Block supports error detection by comparing the D Flip-Flops outputs.

Error Counter Block supports error counting of the error detection block.

High Speed Control Block provides control of the threshold adjustment block, the phase adjustment block, the clock recovery block and the AGC block.

High Speed Information Processing Block retrieves data from the AGC block, from the threshold adjustment block, from the phase adjustment block and from the error counter block.

The present disclosure includes that contained in the appended claims, as well as that of the foregoing description. Although this invention has been described in its preferred form with a certain degree of particularity, it is understood that the present disclosure of the preferred form has been made only by way of example and that numerous changes in the details of construction and the combination and arrangement of parts may be resorted to without departing from the spirit and scope of the invention. Now that the invention has been described,

What is claimed is:

1. A protocol and bit rate independent test system including means for detecting bit errors on a digital communications channel regardless of format or rate, comprising in combination:

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a receiver for receiving an input;

a clock recovery unit;

a threshold sampling circuit for providing at least two threshold detectors for respective two sampling points including at least one static sampling point positioned proximate to the center of an eye pattern and at least one dynamic sampling point, the output of which are sampled by the recovered clock and if the signal passes between the thresholds, an error signal is generated and counted.

2. The protocol and bit rate independent test system as set forth in claim 1, comprising a plurality of the dynamic sampling points and wherein the dynamic sampling points are movable in an array about an eye measurement.

3. The protocol and bit rate independent test system as set forth in claim 2, wherein the array comprises a linear array.

4. The protocol and bit rate independent test system as set forth in claim 2, wherein the array comprises a two-dimensional array.

5. The protocol and bit rate independent test system as set forth in claim 1, wherein said clock recovery unit comprises a variable rate clock recovery unit.

6. The protocol and bit rate independent test system as set forth in claim 1, wherein said receiver comprises an optical receiver and wherein said input comprises an optical input.

7. The protocol and bit rate independent test system as set forth in claim 6, wherein the optical receiver is PIN photodiode based.

8. The protocol and bit rate independent test system as set forth in claim 6, wherein the optical receiver is avalanche photodiode based.

9. The protocol and bit rate independent test system as set forth in claim 1, further including frequency measurement including a high speed prescaler which drives a counter and provides a timebase to a protection switch detection circuit.

10. The protocol and bit rate independent test system as set forth in claim 9, further including a protection switch detection circuit for comparing the counted errors in a given timebase period with a programmable threshold and upon exceeding the threshold, for producing an active protection switch output.

11. The protocol and bit rate independent test system as set forth in claim 1, wherein said threshold sampling circuit comprises a variable threshold sampling circuit.

12. The protocol and bit rate independent test system as set forth in claim 1, further including an error detect and Q measurement processing logic for reading the error signals.

13. The protocol and bit rate independent test system as set forth in claim 1, further including a jitter measurement processing logic.

14. A protocol and bit rate independent test system method for detecting bit errors on a digital communications channel regardless of format or rate, comprising in combination:

receiving an input signal;

recovering the clock from the input signal;

sampling at least two sampling thresholds from the input signal for respective two sampling points including at least one static sampling point positioned proximate to the center of an eye pattern and at least one dynamic sampling point; and

producing an error signal if the input signal passes between the thresholds.

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15. The method as set forth in claim 14, comprising a plurality of the dynamic sampling points and wherein the dynamic sampling points are movable in an array about an eye measurement.

16. The method as set forth in claim 15, wherein the array comprises a linear array.

17. The method as set forth in claim 15, wherein the array comprises a two-dimensional array.

18. The method as set forth in claim 14, wherein the step of recovering the clock from the input signal comprises the step of recovering the clock from the input signal at a variable rate.

19. The method as set forth in claim 14, wherein the step of receiving a signal input comprises the step of receiving an optical signal input.

20. The method as set forth in claim 19, wherein the step of receiving the optical signal input employs an optical receiver.

21. The method as set forth in claim 20, wherein the optical receiver is PIN photodiode based.

22. The method as set forth in claim 21, wherein the optical receiver is avalanche photodiode based.

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23. The method as set forth in claim 14, further including the step of measuring the bit rate to provide a timebase to a protection switch detection circuit.

24. The method as set forth in claim 14, wherein the step of sampling at least two sampling thresholds from the input signal comprises the step of sampling at least two variable sampling thresholds.

25. The method as set forth in claim 14, further including the step of reading the error signals.

26. The method as set forth in claim 25, wherein the step of reading the error signals employs an error detect and Q measurement processing logic.

27. The method as set forth in claim 14, further including the step of comparing the counted errors in a given timebase period with a programmable threshold and upon exceeding the threshold, producing an active protection switch output.

28. The method as set forth in claim 14, further including the step of measuring jitter.

\* \* \* \* \*



US005748672A

**United States Patent** [19]

Smith et al.

[11] Patent Number: **5,748,672**[45] Date of Patent: **May 5, 1998**[54] **SYSTEM FOR MEASURING JITTER IN A NON-BINARY DIGITAL SIGNAL**[75] Inventors: **Marc L. Smith**, Sterling; **Fadi H. Daou**, Milton, both of Mass.[73] Assignee: **CenRad, Inc.**, Concord, Mass.[21] Appl. No.: **514,011**[22] Filed: **Aug. 11, 1995**[51] Int. Cl.<sup>6</sup> ..... **H04B 3/46**[52] U.S. Cl. .... **375/226; 371/1; 364/715.06; 364/732**[58] Field of Search ..... **375/226, 244, 375/371, 376; 371/1; 364/715.06, 732**[56] **References Cited****U.S. PATENT DOCUMENTS**

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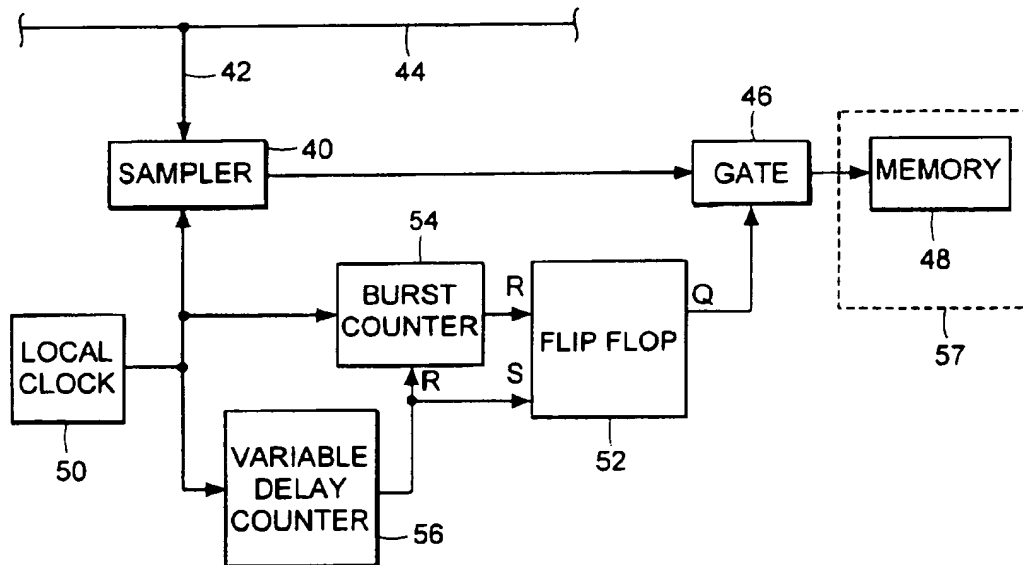
Primary Examiner—Wellington Chin

Assistant Examiner—Congvan Tran

Attorney, Agent, or Firm—Cesari and McKenna, LLP

[57] **ABSTRACT**

To measure various frequency components of the jitter of the deviation of the transition times in a signal on a signal line (44) from nominal bit times, a sampler (40) samples the signal at a rate high enough to determine the transition time with the required resolution. By employing a differentiator (60), test circuitry (FIG. 3B) can detect not only zero crossings but all digital-level transitions. The timings of the maxima of the differentiator output are applied to a Fourier-transform unit (76) that computes jitter-frequency components from a resultant sequence of deviations of the maxima from nominal transition times. Although computation of the lowest jitter-frequency components is necessarily based on a sequence that extends over a correspondingly long signal record, the input of a memory (48) that receives the raw samples from which those transition-time deviations are computed is so gated that the memory (48) receives only infrequently occurring bursts of the sampler's high-sample-rate output when the lower jitter frequencies are to be measured. A memory (48) of only moderate size can therefore be employed despite the necessarily high sample rate and necessarily long record duration.

**15 Claims, 4 Drawing Sheets**

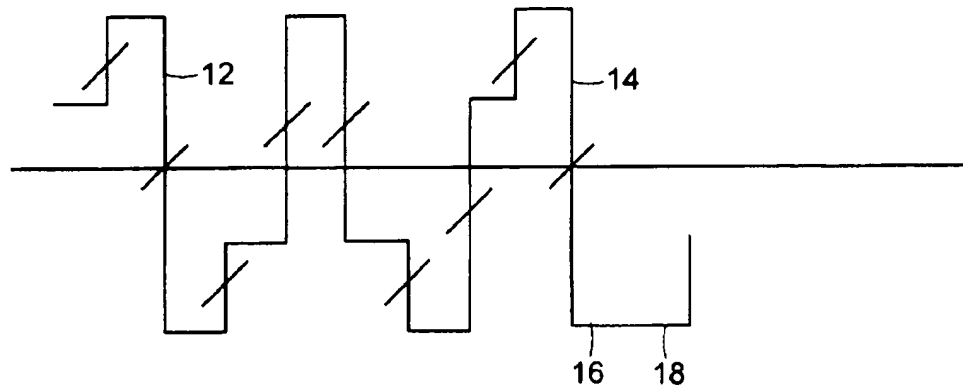


FIG. 1

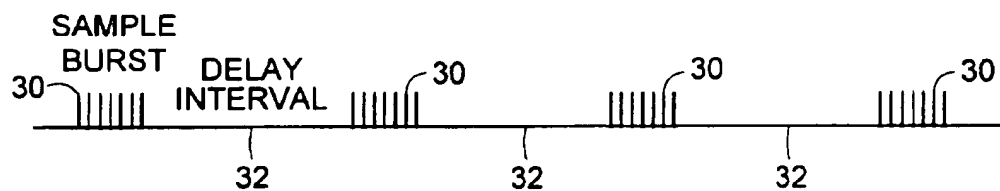


FIG. 2



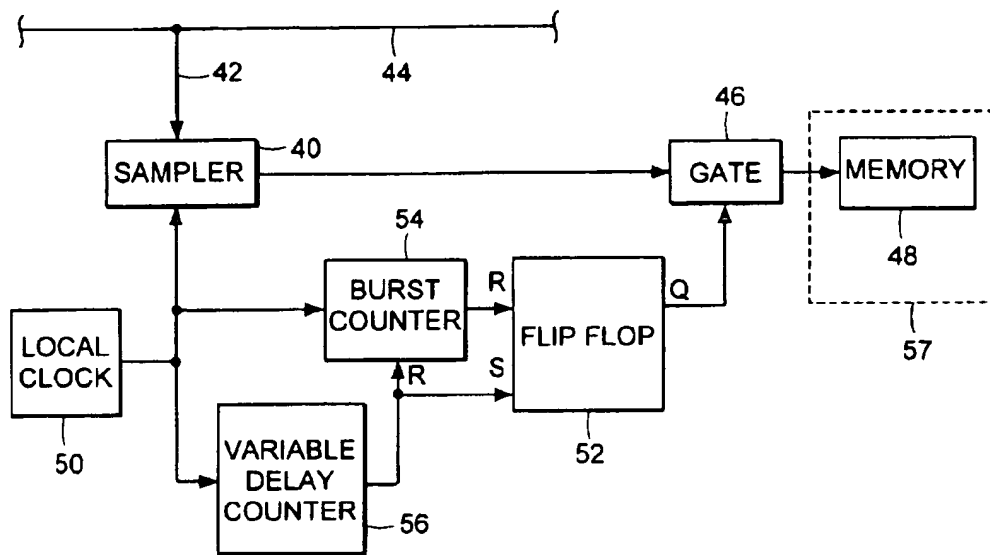


FIG. 3A

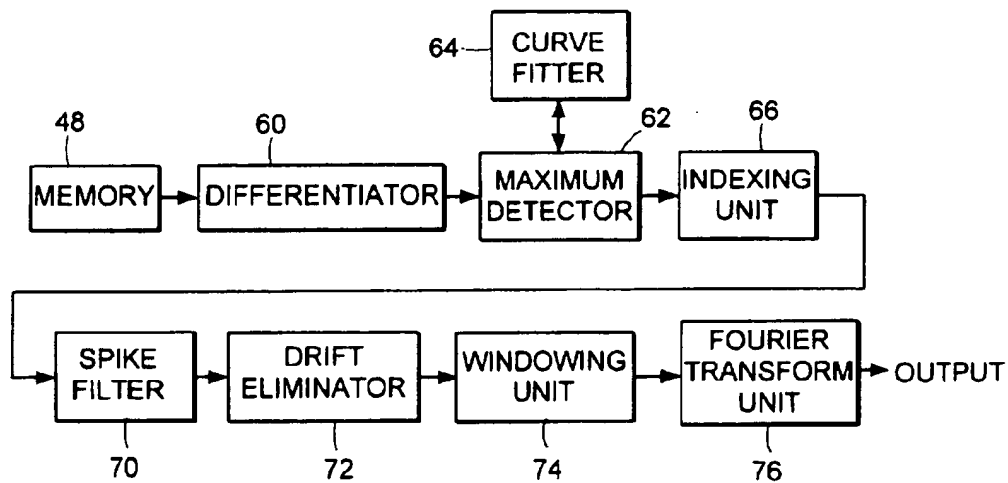


FIG. 3B

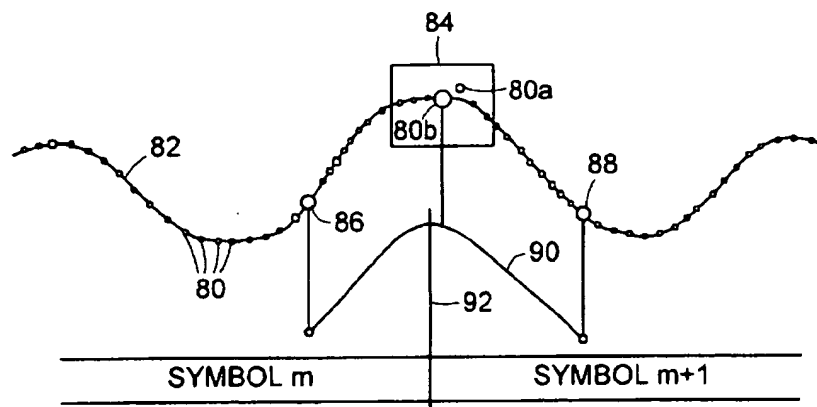


FIG. 4

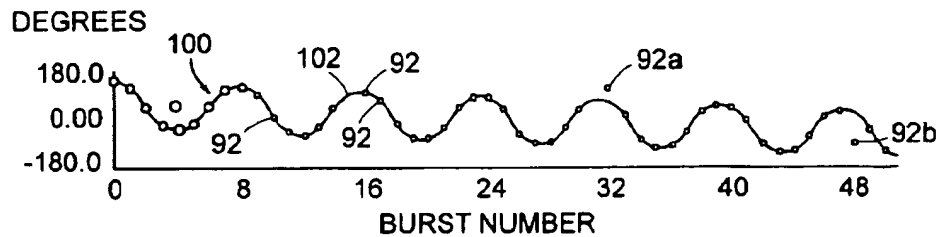


FIG. 5

	SIGNAL SAMPLES/ BURST	SYMBOLS/ BURST	SKIP-INTERVAL (SYMBOLS) (Hz)	JITTER SAMPLE RATE	NUMBER OF BURSTS PER MEASUREMENT
0.15 - 39 Hz	128	2	1022	78.125 Hz	512
0.5 - 62 Hz	255	4	636	125 kHz	256
62 Hz - 8 kHz	255	4	1	16 kHz	256
78 Hz - 20 kHz	128	2	0	40 kHz	512

FIG. 6

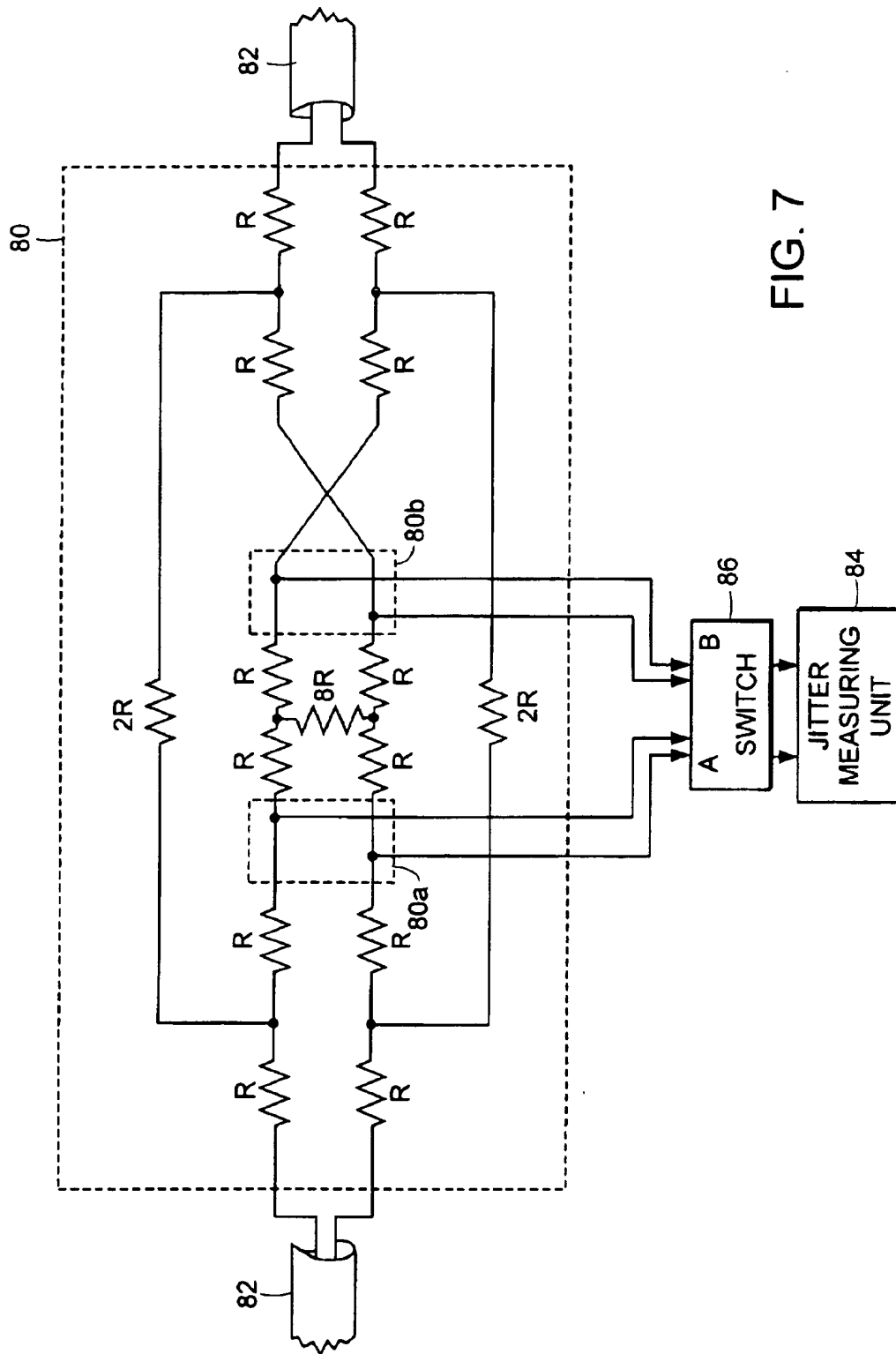


FIG. 7

# SYSTEM FOR MEASURING JITTER IN A NON-BINARY DIGITAL SIGNAL

## BACKGROUND OF THE INVENTION

### A. Field of the Invention

This invention relates to the measurement of clock jitter in self-clocking digital data signals. More specifically, it relates to the sampling of the data signals to recover phase variations of the clock signals embedded therein.

The reception of digital data transmissions requires that the incoming signals be sampled or "strobed" at periodic, precise intervals to sense the values of the signals at those times. For example, a simple binary data signal should be sampled in the middle of each bit cell to determine whether the bit is a 1 or a 0. Obviously the sampling, which is timed by a clock signal, must be synchronized with the data signal if errors are to be minimized.

Usually self-clocking schemes are used in the transmission of data. The clock signal is, in essence, embedded in the data signal. It is recovered at the receiver to control a local clock whose output is used to strobe the incoming data signal and thereby detect the data. Thus the timing of the clock signal relative to the data signal is fixed at the transmitter and is not affected by the characteristics of the path from the transmitter to the receiver. Accordingly, if the characteristics of the transmitter or the path change, the relative clock-data timing will not change. The phase-lock-loop that controls the local clock will adjust the phase of the clock so as to preserve the proper clock timing relative to the data.

However, if the phase of the received data signal varies too rapidly, the phase-lock loop will be unable to adjust the local clock fast enough, to follow the corresponding changes in the phase of the embedded clock signal and errors in data detection will result. For this reason standards have been promulgated, governing the amount and rate of phase change ("phase jitter") that are allowed in the transmission paths. The present invention is directed to an improved system for ascertaining the phase jitter to determine compliance with the applicable standard.

### B. Description of Related Art

Prior systems sense the zero crossings of the data signals to determine the phases of the embedded clock signals. However, this requires that the transitions involve zero crossings and, furthermore, that they be symmetrical with respect to the crossings. For example, with the 2B1Q format used in ISDN communications, most of the signal transitions will not meet this criterion. Systems using this ISDN format may transmit at a rate of 80,000 symbols/second, while a jitter standard for the 2B1Q format may cover jitter frequency components from 0.15 Hz to 20k Hz. Accordingly the use of zero-crossing detection to ascertain jitter magnitude will usually not provide a high enough sampling rate to measure jitter components in the mid to upper portions of this frequency range unless normal transmissions are interrupted and a predetermined pattern of symbols is transmitted.

Accordingly it is an object of the invention to provide an improved method and apparatus for measuring phase jitter in digital data signals. A more specific object of the invention is to provide accurate measurements of phase jitter in signals transmitted during normal operation of a monitored system. A further object is to provide accurate measurements of phase jitter over a wide range of jitter frequencies. Yet another object of the invention is to provide accurate mea-

surement of phase jitter in signals propagating in either direction over a transmission line.

## DESCRIPTION OF THE INVENTION

### A. BRIEF SUMMARY OF THE INVENTION

In accordance with the invention we sense transitions in a data signal by differentiating the signal and using the maximum absolute value of the derivative as the timing mark for each transition. Thus, each transition is eligible for use in measuring phase jitter and the high-frequency components of the jitter are easily within the range of the measuring system.

The system operates digitally, by sampling the data signal at a relatively high rate, e.g. 64 samples/symbol and using these samples in computing the derivative. Together with a curve-fitting procedure, described below, this provides sufficient resolution in locating the derivative maxima.

The invention can also be used to measure phase jitter in signals propagating in both directions over a transmission line. For this purpose we insert a directional coupler into the transmission line. The coupler has two output ports, one for signals travelling in one direction and the other for signals travelling in the opposite direction. The jitter-measuring unit described herein can be switched between the two ports to measure the jitter for signals travelling in the respective directions.

FIG. 1 illustrates a fragment of a signal representing a sequence of symbols transmitted with the 2B1Q format. The depicted waveform is idealized in that the various transitions in voltage level are indicated as occurring instantaneously. In fact, however, because of bandwidth limitations in the circuitry that generates the waveforms and in the transmission lines over which they are propagated, each transition occurs over a finite time interval.

In order to provide uniformity in sensing the timing of each transition, the occurrence of the transition is usually defined as the midpoint between the starting and ending points of the transition. The midpoint, in turn, can be sensed by means of a zero-crossing detector, but only for those transitions for which the zero axis is the midpoint. In FIG. 1 only the transitions indicated at 12 and 14 have this characteristic. The remaining transitions either do not cross the zero axis or cross it but are asymmetrical with respect to the axis. Indeed, the consecutive symbols indicated at 16 and 18 have the same voltage level and thus have no intervening voltage transition.

Thus prior systems which are based on the sensing of zero axis crossings may, because of the intervals often encountered between usable crossings, miss high-frequency phase jitter components which are covered by the applicable standards. It will be apparent that with the signal sequence depicted in FIG. 1, and given a data rate of 80,000 symbols/second, high-frequency phase jitter components will not be detected if only symmetrical zero axis crossings are used for measurement of the timing of signal transitions.

On the other hand, with our invention, which uses the occurrence of the maximum absolute value of the slope, i.e. rate of change of signal voltage, as the indication of the midpoint of each transition, every transition can be used for the measurement of transition timing. The resulting determination of the timing of a transition provides a single sample of the phase jitter. For any frequency component in the phase jitter, the system must obtain enough jitter samples to ascertain the magnitude of that component with a reasonable degree of accuracy. In the high frequency portion of

the measurement range, e.g. from 2,000 Hz to 20 kHz, 500 samples of the phase jitter will provide an accurate characterization of the magnitude of the jitter components at the frequencies involved. At the low frequency end of the spectrum, i.e. 0.15 Hz, jitter samples taken over approximately a single cycle of that component will accurately characterize the magnitude of the jitter. However, with the sampling rate provided for the high-frequency components, there will be an inordinately large number of samples, with corresponding demands on memory capacity and computation time.

We therefore sample the data signal in accordance with a burst arrangement. As shown in FIG. 2, sampling of the data signal is performed in bursts 30 separated by skip intervals indicated at 32. The bursts and skip intervals are synchronized to a local clock and the total length of a sample burst, plus a delay period is an integral number of symbols. The number of samples in each burst is sufficient to encompass multiple symbols increases the likelihood that at least one signal transition will occur during each burst. In each burst, the timing of the transition having the greatest absolute slope is selected as a jitter sample.

The burst length and the length of the skip interval depend on the range of jitter frequencies involved in the measurement. For measurement of the higher frequency components of the phase jitter a relatively short or even zero-length skip interval is required in order to provide a sufficiently high sampling rate for the phase jitter. On the other hand, at low frequencies, where the sampling rate is not an imposing limitation, we use a relatively long skip interval to conserve system resources as noted above. Specifically we have found that the jitter-frequency spectrum of 0.15 Hz to 20 KHz can be divided into four ranges, each having a different skip interval. These burst and the sampling sequences relating thereto are set forth in FIG. 6, assuming a symbol rate of 80,000/sec in the monitored signal and a sampling rate of 64 samples/symbol. For example, over the jitter frequency range 0.5-39 Hz we use a burst length of 128 samples, or two symbols, and a skip interval of 1022 symbols. This provides a jitter sample rate of 78.125, slightly in excess of the minimum sampling rate for the upper level of the frequency range. A total of 512 sampling bursts, i.e. jitter samples, are used for this measurement.

Similar measurement parameters are provided in FIG. 6 for three further jitter frequency ranges extending to 20 kHz. In the uppermost range, 78 Hz to 20 kHz, the skip intervals is zero and each sampling burst thus immediately succeeds the preceding burst.

### B. BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature of the invention, reference should be had to the following detailed description taken in connection with the accompanying drawings, in which:

FIG. 1 depicts an idealized signal waveform in the 2B1Q format;

FIG. 2 depicts a succession of sampling bursts used in sampling signals in accordance with the invention;

FIG. 3A is a block diagram of a signal sampling unit incorporated in a jitter-measuring system embodying the invention;

FIG. 3B is a block diagram of a signal analysis unit incorporated in the jitter-measuring system;

FIG. 4 illustrates a waveform of the time derivative of a monitored signal and the application of the invention to the

waveform by the signal analysis unit to ascertain the timing of transition in the monitored signal;

FIG. 5 is a waveform of the phase of the monitored signal as measured by the signal analysis unit;

FIG. 6 is a chart of the signal-sampling sampling sequences for the various frequency ranges in the jitter spectrum; and

FIG. 7 is a diagram of a system for measuring phase jitter in signals passing in either direction over a transmission line.

### C. DETAILED DESCRIPTION OF THE INVENTION

With reference to FIG. 3A, a sampler 40 which is connected to a tap 42 on a transmission line 44 provides a sequence of digital representations of the instantaneous signal voltage levels on the line. These digital signals are passed by a gate 46 to a random access memory 48 where they are accumulated for subsequent processing as described below. Operation of the sampler 40 is timed by the output of a local clock 50. The clock 50 is highly stable and has an output frequency as close as is practicable to an integral multiple of the symbol rate  $f_0$  of the signals transmitted over the line 44. We have found that a multiple of 64 provides the desired resolution in sampling of the monitored signals when the interpolation arrangement described herein is used. The gate 46 is controlled by the output of a flip-flop 52 whose state is controlled by the outputs of a burst counter 54 and a skip counter 56, both of which count the output pulses of the clock 50.

The burst counter 54 has a capacity corresponding to a time length corresponding to multiple symbols in the monitored signal. It is adjustable to provide for different burst lengths according to the jitter frequency range involved in the measurement, as described above. The adjustments of the skip counter 56 are limited to counter capacities corresponding to integral numbers of symbols, i.e. integral multiples of 64 samples. Overflow of the counter 56 sets the flip-flop 52 so that its output enables the gate 46 and at the same time resets the counter 54. The gate 46 thereupon passes samples from the sampler 40 to the memory 48 until the counter 54 reaches its maximum count, at which point the counter 54 output resets the flip-flop 52, thereby disabling the gate 46.

As pointed out above, the burst of samples passed by the gate 46 during each of these cycles of the counters 54 and 56 ultimately provides one sample of the timing of the monitored signal. A sufficient number of bursts are passed to provide the requisite number of samples for a selected frequency range of the phase jitter in the monitored signal.

The capacities of the burst counter 54 and the skip counter 56 are thus changed to provide different burst lengths and timings between the bursts (i.e. skip intervals) and thereby provide for measurement of the phase jitter components in the respective frequency ranges. At the highest frequency range the capacity of the counter 56 is equal to that of the counter 54 so that continuous bursts of samples are fed to the memory 48.

It will be apparent that the gate 46, counters 54 and 56 and flip-flop 52 can be implemented in hardware or their functions can be provided by a digital computer 57 of which the memory 48 is a component.

After the samples for a measurement have been accumulated in the memory 48, the computer 57 executes a series of software routines to process the samples and thereby provide the desired phase jitter measurements. FIG. 3B

illustrates these routines as blocks of a corresponding hardware diagram. Specifically the samples from each burst are applied to a differentiator 60 whose output is a series of samples of the time derivative of the monitored signal. The output of the differentiator 60 is applied to a maximum

detector 62 which calculates the position of the absolute maximum slope of the signal during the burst. More specifically, the differentiator 60 simply calculates the differences between the values of successive signal samples to provide the derivative samples, indicated at 80 (FIG. 4), that define a derivative curve 82. The maximum detector 62 then selects a primary reference point which is, in essence, a rough determination of an absolute maximum of the derivative curve 82.

To determine the position of each primary reference point, we prefer to use a moving "window", as indicated at 84 in FIG. 4, encompassing a number of samples, e.g. 7. The window 84 is moved through the sample set in each burst and the sample values in the window are summed. The primary reference point is the central sample in the window when the sum has a maximum (or minimum) value. This arrangement diminishes the effects of noise in selecting the primary reference point. For example, if the values of individual samples were to be used in selecting the primary reference point, the sample 80a would be selected, whereas the sample 80b, which is at the center of the window 84 at the depicted position of the window, is clearly closer to a maximum of the curve 82.

In general the primary reference point will not be the true position of a maximum of a derivative curve 82. For example, errors are caused by noise and by the spacing between adjacent signal samples. We therefore prefer to use a curve-fitter 64, which reduces this error. A quadratic curve is fitted to the primary reference point and to samples preceding and following that sample. The latter two samples may, for example, be spaced from the primary reference point by twelve sample intervals, as indicated at 86 and 88 in FIG. 4. These three samples 80b, 86 and 88, fix the coefficients of the quadratic expression.

The system derives the first two coefficients and uses them in differentiating the expression to find the position of the maximum. Thus, with the illustrated curve 82 and the maximum encompassed by the window 84, a quadratic curve 90 fits the samples 80b, 86 and 88. This curve has a maximum at 92, which is taken as a maximum of the derivative and thus the location, i.e. timing, of the signal transition involved in the calculation.

As an example of the advantages to be gained from the foregoing procedure, measurements were taken which provided the illustrated derivative curve 82. If the maximum sample value is taken as the point of the derivative maximum, i.e. the position of the sample 80a, there was an error of 32.6 degrees. The selection of the primary reference point 80b as the maximum reduced the error to 17.6 degrees. On the other hand, selection of the maximum point of the quadratic approximation, i.e. the position indicated at 92, reduced the error to 0.3 degrees.

As noted above, each burst of signal samples is of sufficient duration to encompass multiple transitions in the monitored signal. In an illustrative system the burst durations are as set forth in FIG. 6. Thus, when making a measurement in the jitter-frequency range 62 Hz to 8 kHz there will be four possible points in each burst where a signal transition having the absolute maximum slope in that burst may occur. To facilitate the development of a jitter waveform from the transition information provided by the maxi-

mum detector 62, the maxima in all the bursts must be referenced to the same position within the bursts. That is, with up to four possible transition positions in each burst, one of those positions is selected as a reference and the maxima that occur at or in the neighborhood of the other three positions are indexed to that position by adding or subtracting the nominal phase differences between those positions and the reference position.

Any one of the four transition positions can be selected as the reference position. However, since indexing of the positions to a common reference is a source of error, we prefer to select, as the reference, the position involving the greatest number of derivative maxima. Accordingly, after the maxima have been identified by the maximum detector 62, the system uses an indexing unit 66 to essentially calculate a histogram of the number of selected maxima in the neighborhood of each of the four nominal transition positions. It then selects as the reference position the position involving the greatest number of maxima and indexes all the other maxima to that burst position. A similar arrangement is followed in the frequency ranges in which two signal transitions are encompassed by each sample burst.

After they are indexed to a single burst position, the selected transitions define a curve of which the curve 100 in FIG. 5 is an example. This curve has a sinusoidal component and an overall slope. The sinusoidal component is a graphical representation of the phase jitter and the slope represents drift, mainly due to the difference in frequency between the clock 50 (FIG. 3A) and the clock (not shown) that is used in generating the monitored signal. The waveform may have some impulse noise as indicated by the samples 92a and 92b and it is therefore passed through a spike filter 70 (FIG. 3B) that will tend to smooth out high frequency spikes.

Also, in some cases a burst may contain a sequence of symbols that does not provide sufficiently good transitional information to select a maximum. In such cases a transition will be missing from the curve 100 as indicated, for example, at 102. A pseudo transition is then inserted by interpolation, preferably linear interpolation.

Next the drift is removed from the waveform 100 by a drift eliminator 72 (FIG. 3B). The drift eliminator calculates the slope of the ramp of the curve by first determining average values of the bursts in the first and last portions of the waveform, e.g. the first quarter and the last quarter. The difference between the two values is averaged over the number of bursts to give the average drift. Then an accumulated drift is subtracted from the waveform to "level" the waveform. The average value of the entire waveform is then calculated and also subtracted from the waveform, thereby leaving only the AC components, i.e. the jitter.

Returning to FIG. 3B, a Fourier transform can be applied to the resulting waveform to ascertain the frequencies and amplitudes of the various components in the waveform. Since the waveform has a finite length and since the measurement system is not coherent with the jitter frequencies, a transform at this juncture will generally produce spurious side lobes in the output. Accordingly, we prefer to pass the waveform through a windowing unit 74 which applies a cosine-bell window to the waveform to force the ends of the waveform to zero amplitude. The windowed waveform is then passed to a FFT-unit 76 which performs the Fourier transform to produce the output of the system.

The foregoing procedure is applied separately in the respective frequency bands as explained above. That is, for each band a different signal-sampling burst length and burst

rate are used as set forth above. The invention thus provides a high degree of accuracy without resort to undue storage and processing time for determination of the low-frequency jitter components.

In FIG. 7 we have illustrated a system for monitoring phase jitter of signals propagating in either direction over a transmission line having a characteristic impedance  $R$ . A directional coupler indicated generally at 80 is inserted in the transmission line. The illustrated coupler 80 is a resistive network configured as shown, with the individual resistors preferably having the resistance values shown so as to match the transmission impedance. The coupler also has a pair of sampling ports 80a and 80b, which, respectively, provide replicas of the signals propagating in opposite directions on the transmission line 82.

A jitter measuring unit 84, of the type illustrated in FIGS. 3A and 3B, is selectively connected to the ports 80a and 80b, for example, by a switch 86. Thus, connecting the switch 86 first in one position and then the other position, one may monitor the phase jitter in signals propagating in one direction over the line 82 and then in signals propagating in the opposite direction.

The terms and expressions which have been employed are used as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described or portions thereof, but it is recognized that various modifications are possible within the scope of the invention claimed.

What is claimed is:

1. A jitter measuring system for measuring phase jitter of the transitions in a multiple-level digital signal, the system comprising:

A. a local clock,

B. sampling means for sampling the signal in synchronism with the local clock at a rate substantially greater than the symbol rate in the signal, thereby to provide a series of digital signal samples, each of which represents a value of the signal,

C. derivative means for

- 1) processing the signal samples to obtain a series of samples of the time derivative of signal, and
- 2) processing the derivative samples to provide a series of values of the timing of absolute maxima of the derivative, the timing values being samples of the waveform of the phase jitter.

2. The system defined in claim 1 in which the sampling means samples the signal in spaced-apart bursts, and wherein the timing values are samples of the low-frequency components of the phase jitter.

3. The system defined in claim 1 in which the sampling means samples the signal in consecutive sets of bursts, each set having a different burst rate, whereby the timing values obtained from the respective burst sets are samples of different ranges of frequency components of the phase jitter.

4. The system defined in claim 3 in which the derivative means includes:

A. means for identifying for each burst the derivative sample closest to the absolute maximum slope of the signal, and

B. means for fitting a quadratic curve to a set of samples including the closest sample and calculating the timing of the maximum of the curve to provide a sample of the jitter waveform.

5. The system defined in claim 3 in which the derivative means

A. passes a multiple-sample window along the series of samples of the time derivative in each burst,

B. ascertains the position of the window when the sum of the values of the samples contained therein corresponds with an absolute maximum value of the time derivative, and

C. selects the central sample in the window at that position as a primary reference point of the absolute maximum.

6. The system defined in claim 5 further including means for

A. fitting a quadratic curve to a set of samples including the primary reference point and a pair of samples preceding and following the primary reference point, and

B. calculating the maximum of the curve provide a sample of the jitter waveform.

7. The system defined in claim 1 including transform means for generating a Fourier transform of the curve represented by the timing values, thereby to provide a spectrum of the phase jitter.

8. The system defined in claim 7 in which the transform means includes:

means for processing the jitter waveform samples to remove therefrom any variation in the timing values due to a frequency difference between the signal transitions and the local clock.

9. The system defined in claim 1 including:

A. a directional coupler connected in a transmission path of digital signals whose phase jitter is to be measured, the directional coupler having a pair of output ports providing replicas of the signals passing in the respective directions in the transmission path, and

B. means for connecting the sampling means alternatively to the first and second output ports, thereby to selectively measure the phase jitter and the signals passing in the respective directions.

10. A jitter measuring system for measuring phase jitter of the transitions in a multiple-digital signal, said system comprising a:

A. local clock;

B. sampling means for sampling the signal in synchronism with the local clock at a rate substantially greater than the symbol rate in the signal, thereby to provide a series of digital signal samples, each of which represents a value of the signal, the sampling means sampling the signal in bursts, each of which encompasses multiple transitions of the signal;

C. derivative means for:

1. processing the signal samples to obtain a series of samples of the time derivative of the signal; and
2. processing of derivative samples to provide a series of timing values, each of which represents the timing of the absolute maximum of the derivative in a burst, the timing values being samples of the waveform of the phase jitter.

11. The system defined in claim 10 in which the derivative means:

A. passes a multiple-sample window along the series of samples of the time derivative in each burst,

B. ascertains the position of the window when the sum of the values of the samples contained therein corresponds with an absolute maximum value of the time derivative, and

C. selects the central sample in the window at that position as a primary reference point of the absolute maximum.

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12. A system defined in claim 11 further including means for:

A. fitting a quadratic curve to a set of samples including the primary reference point and a pair of samples preceding and following the primary reference point, and

B. calculating the maximum of the curve to provide a sample of the jitter waveform.

13. A method of measuring phase jitter of the transitions in a digital signal, the method comprising the steps of:

A. sampling the signal at a rate substantially greater than the symbol rate in the signal to provide a series of digital signal samples, each of which represents a value of the signal.

B. obtaining from the signal samples a series of samples of the time derivative of the signal, and

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C. processing the derivative samples to provide a series of timing values representing the timing of absolute maxima of the derivative samples, the timing values being samples of the waveform of the phase jitter.

14. The method defined in claim 13 in which:

A. the signal is sampled in bursts, each of which encompasses multiple transitions of the digital signal, and

B. in the processing step, the absolute maximum of the derivative samples in each burst is ascertained to provide a sample of the waveform of the phase jitter.

15. The system defined in claim 14 in which the digital signal is sampled in sets of bursts, each set having a different burst rate, whereby the timing values obtained from the respective sets of bursts are samples of different ranges of frequency components of the phase jitter.

\* \* \* \* \*



UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,748,672  
DATED : May 5, 1998  
INVENTOR(S) : Marc L. Smith, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, item [73] Assignee, should read—GenRad, Inc., Concord, MA--.

Signed and Sealed this  
Twenty-fifth Day of August, 1998



Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks



US006622256B1

(12) **United States Patent**  
Dabral et al.

(10) Patent No.: **US 6,622,256 B1**  
(45) Date of Patent: **Sep. 16, 2003**

(54) **SYSTEM FOR PROTECTING STROBE GLITCHES BY SEPARATING A STROBE SIGNAL INTO POINTER PATH AND TIMING PATH, FILTERING GLITCHES FROM SIGNALS ON POINTER PATH THEREOF**

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(73) Assignee: Intel Corporation, Santa Clara, CA (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/539,666

(22) Filed: Mar. 30, 2000

(51) Int. Cl.<sup>7</sup> ..... G06F 1/04

(52) U.S. Cl. .... 713/600; 713/401; 365/193

(58) Field of Search ..... 713/400, 401,  
713/500, 501, 503, 600; 327/141, 153,  
147, 158, 269; 365/191, 193

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Primary Examiner—Thomas Lee

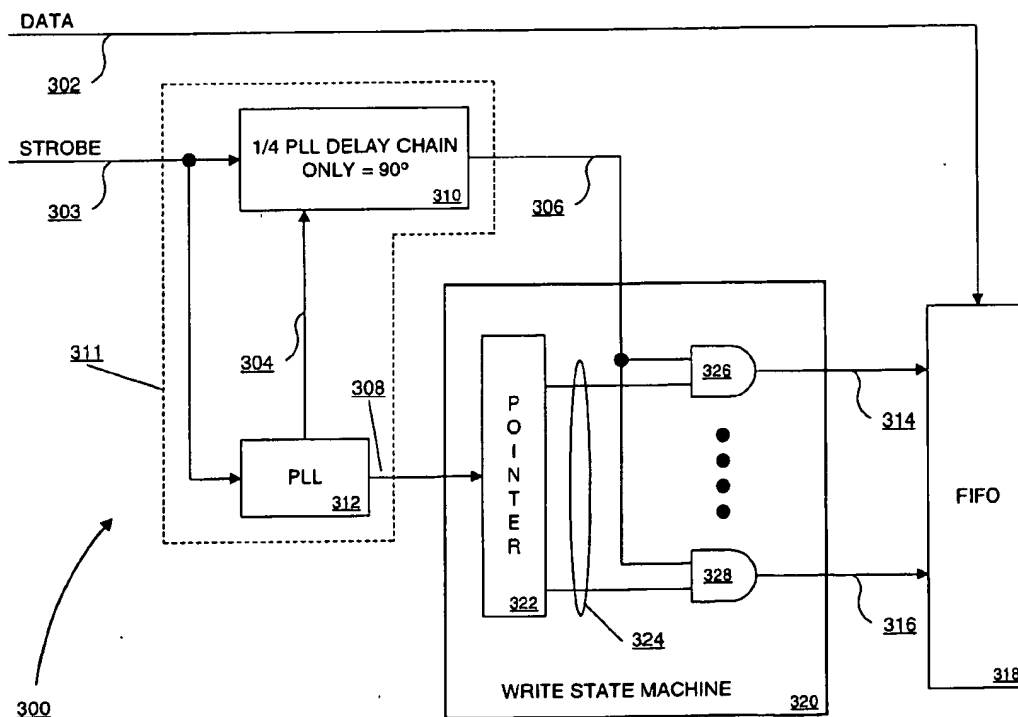
Assistant Examiner—Thuan Du

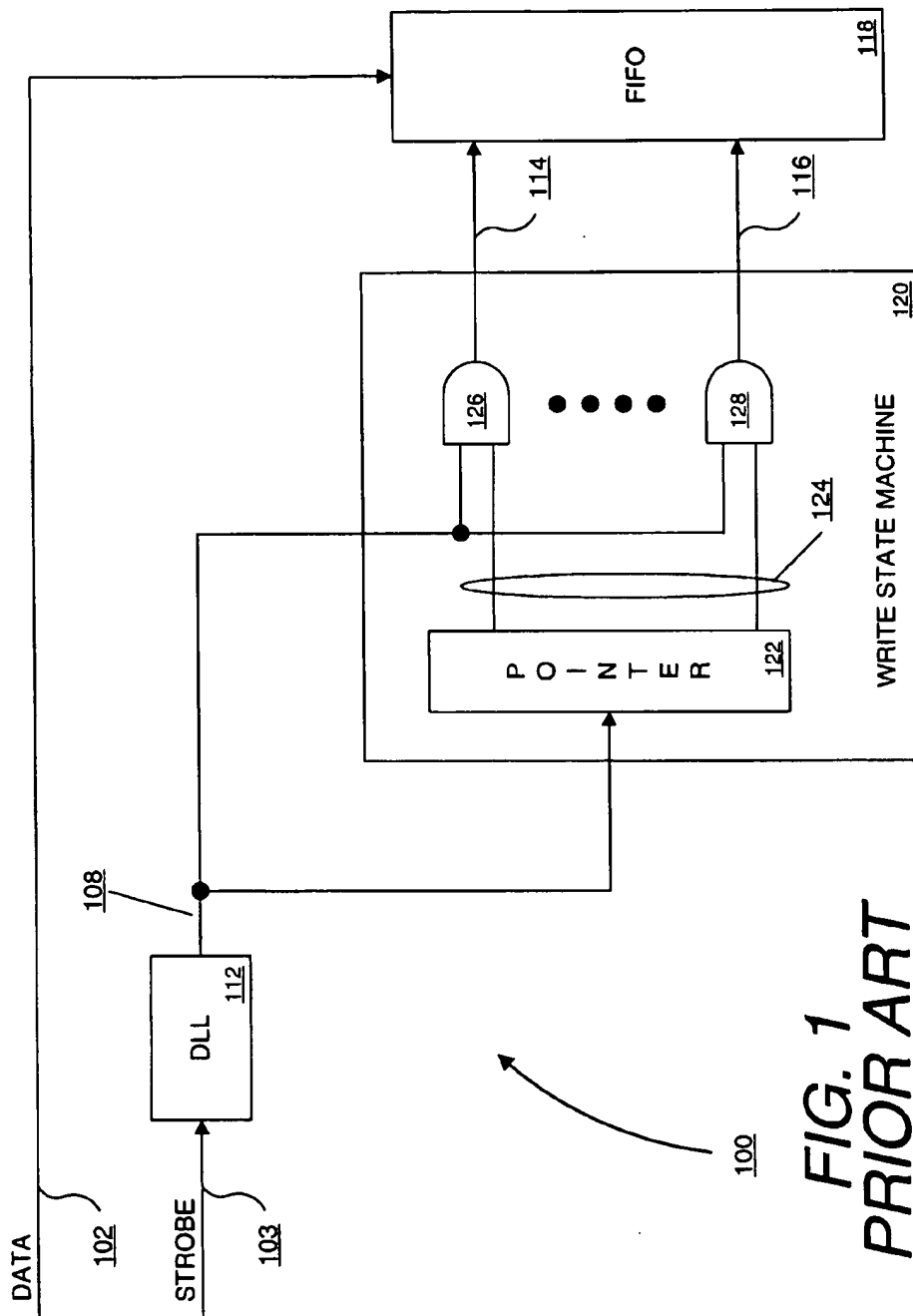
(74) Attorney, Agent, or Firm—Peter Lam

(57) **ABSTRACT**

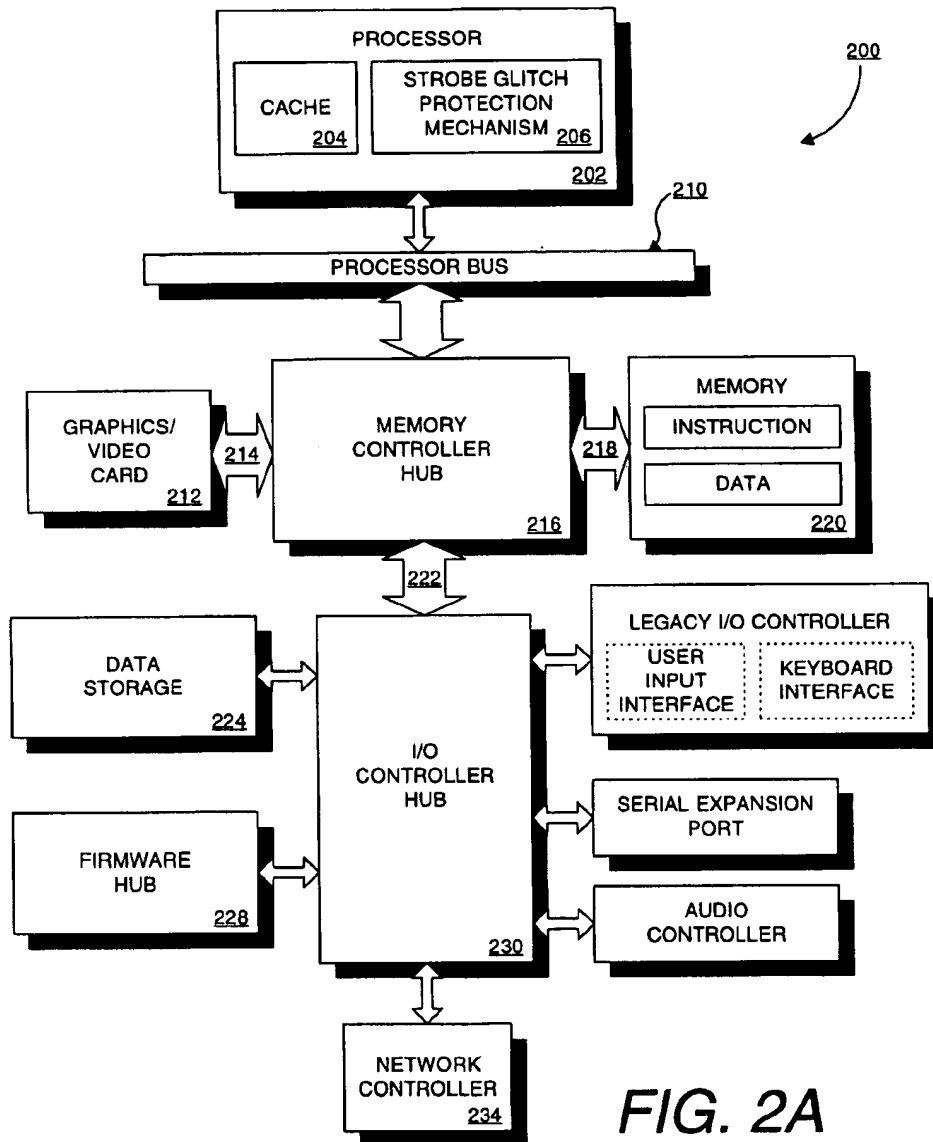
A method and apparatus for a strobe glitch protection mechanism for a source synchronous I/O link. One method of the present invention comprises separating a transfer clock having a plurality of transfer clock edges into a pointer path and a timing path. Glitches are filtered from signals on said pointer path. The pointer path and the timing path are coupled to generate latch enable signals to latch data bits.

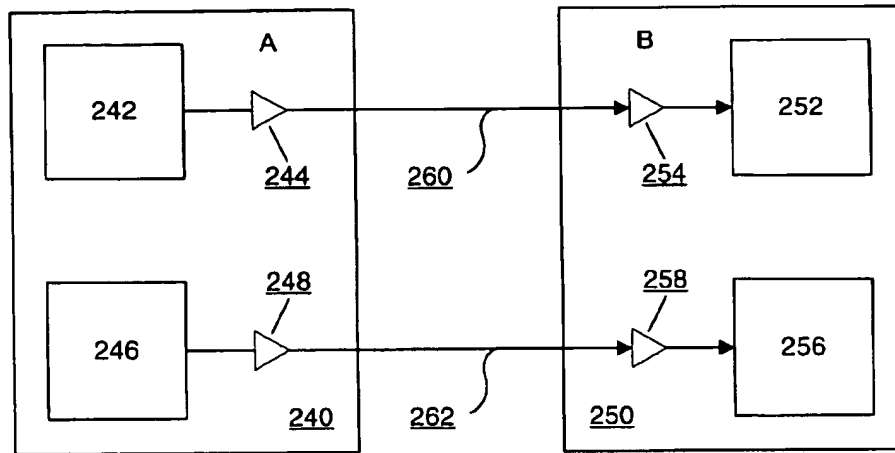
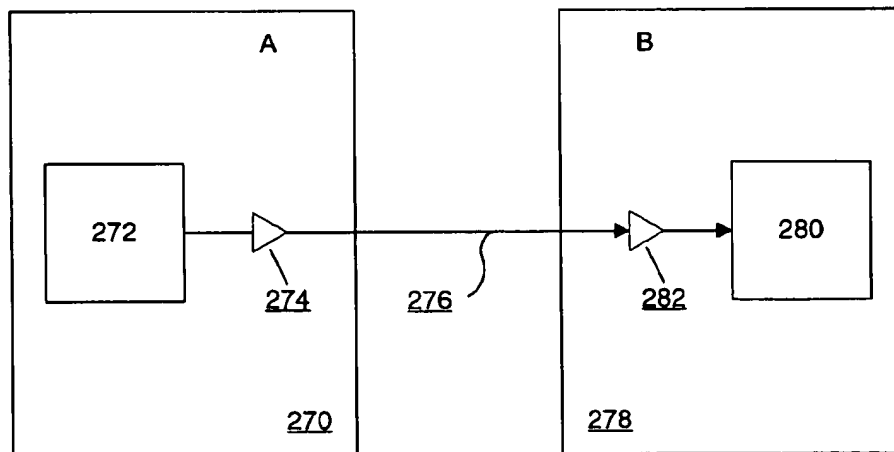
**33 Claims, 10 Drawing Sheets**





**FIG. 1**  
**PRIOR ART**

**FIG. 2A**

*FIG. 2B**FIG. 2C*

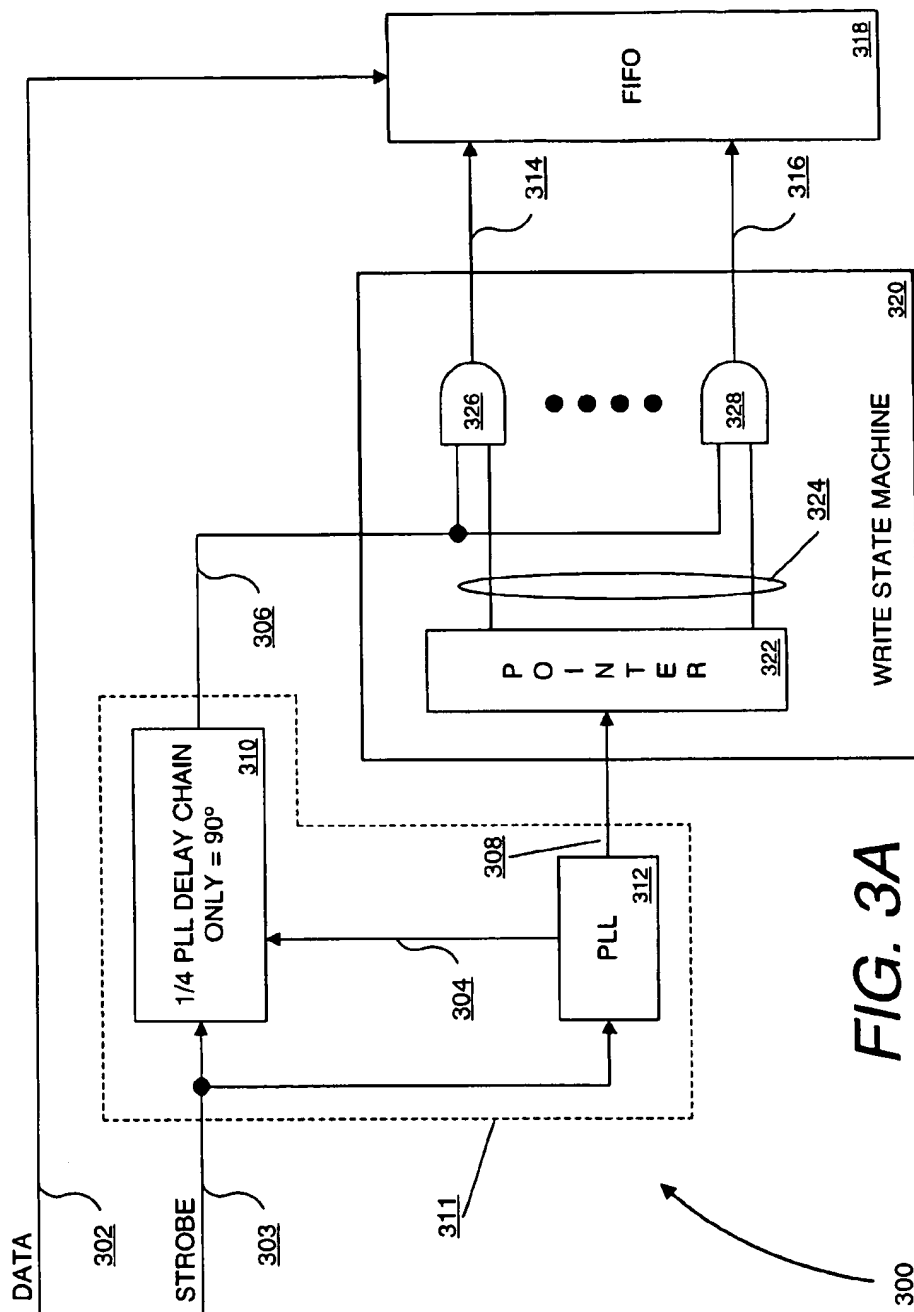


FIG. 3A

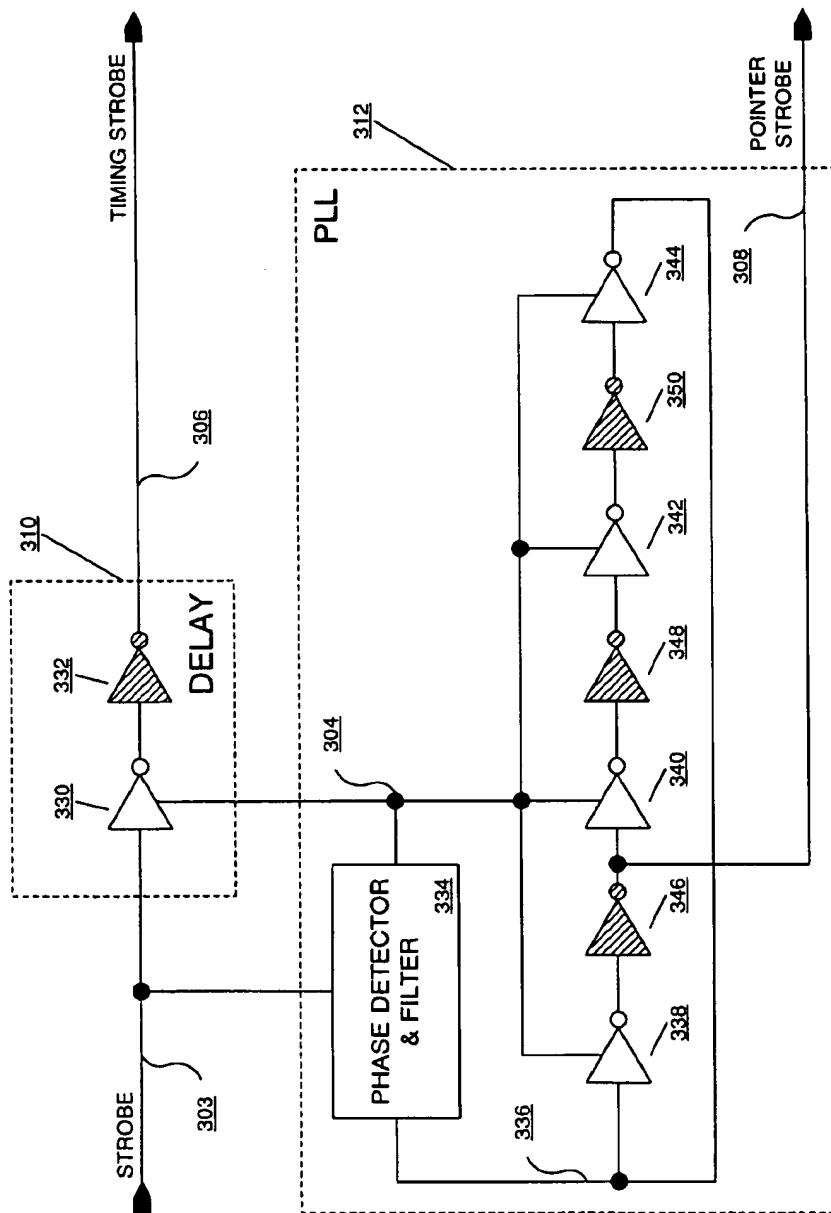


FIG. 3B

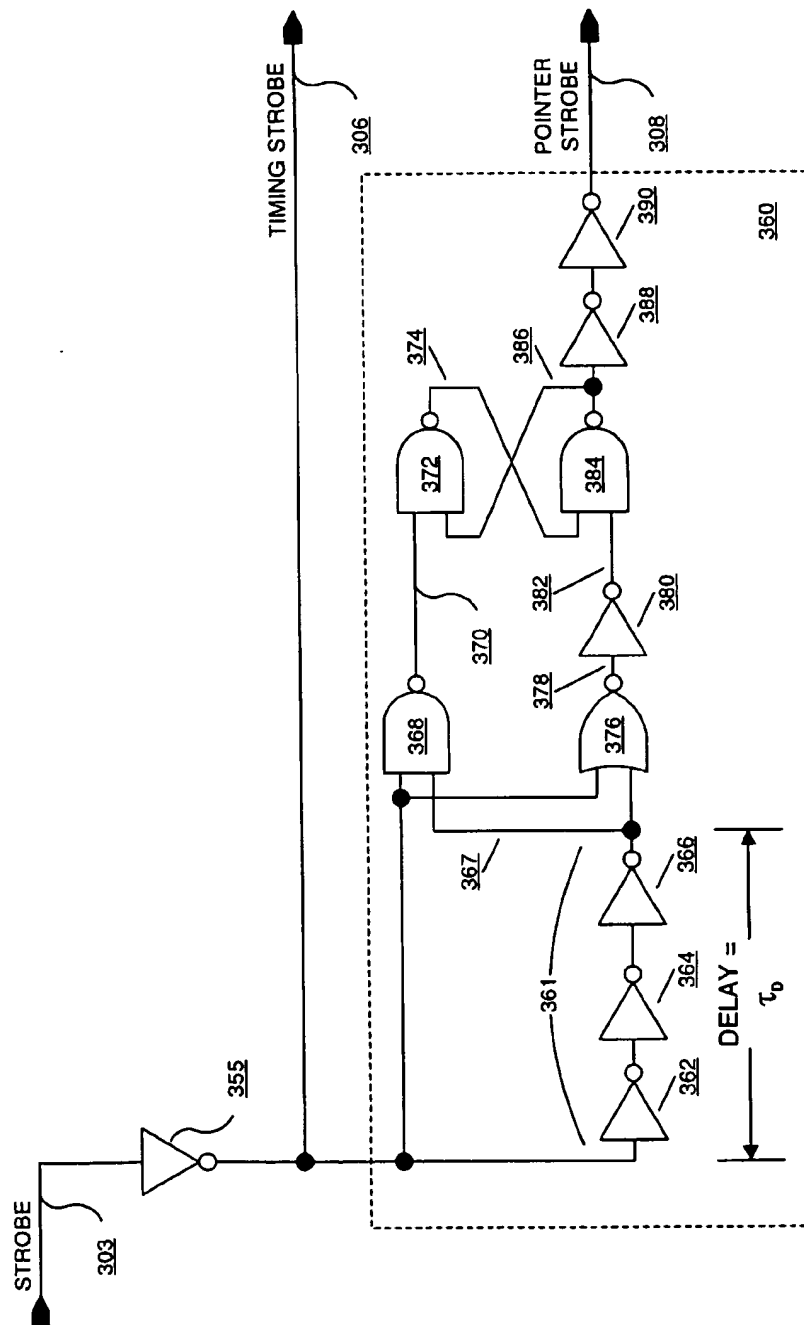
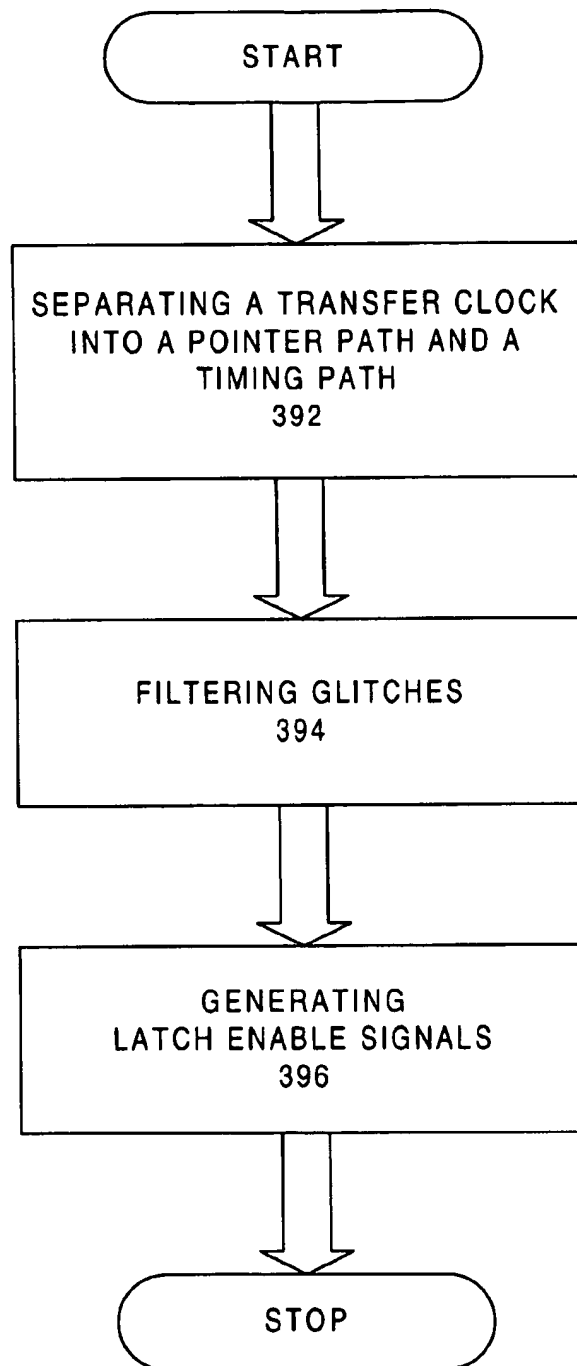


FIG. 3C



**FIG. 3D**

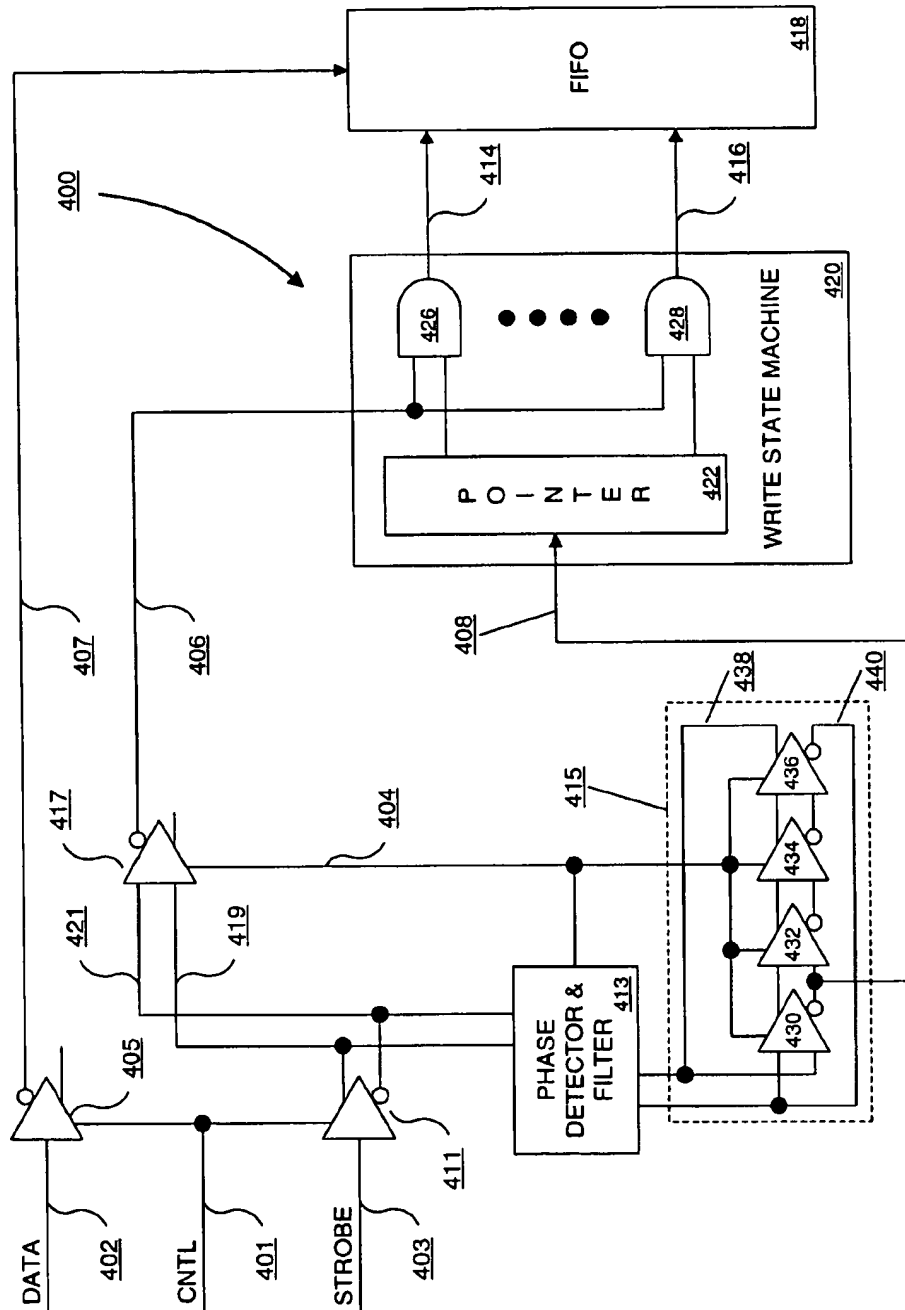
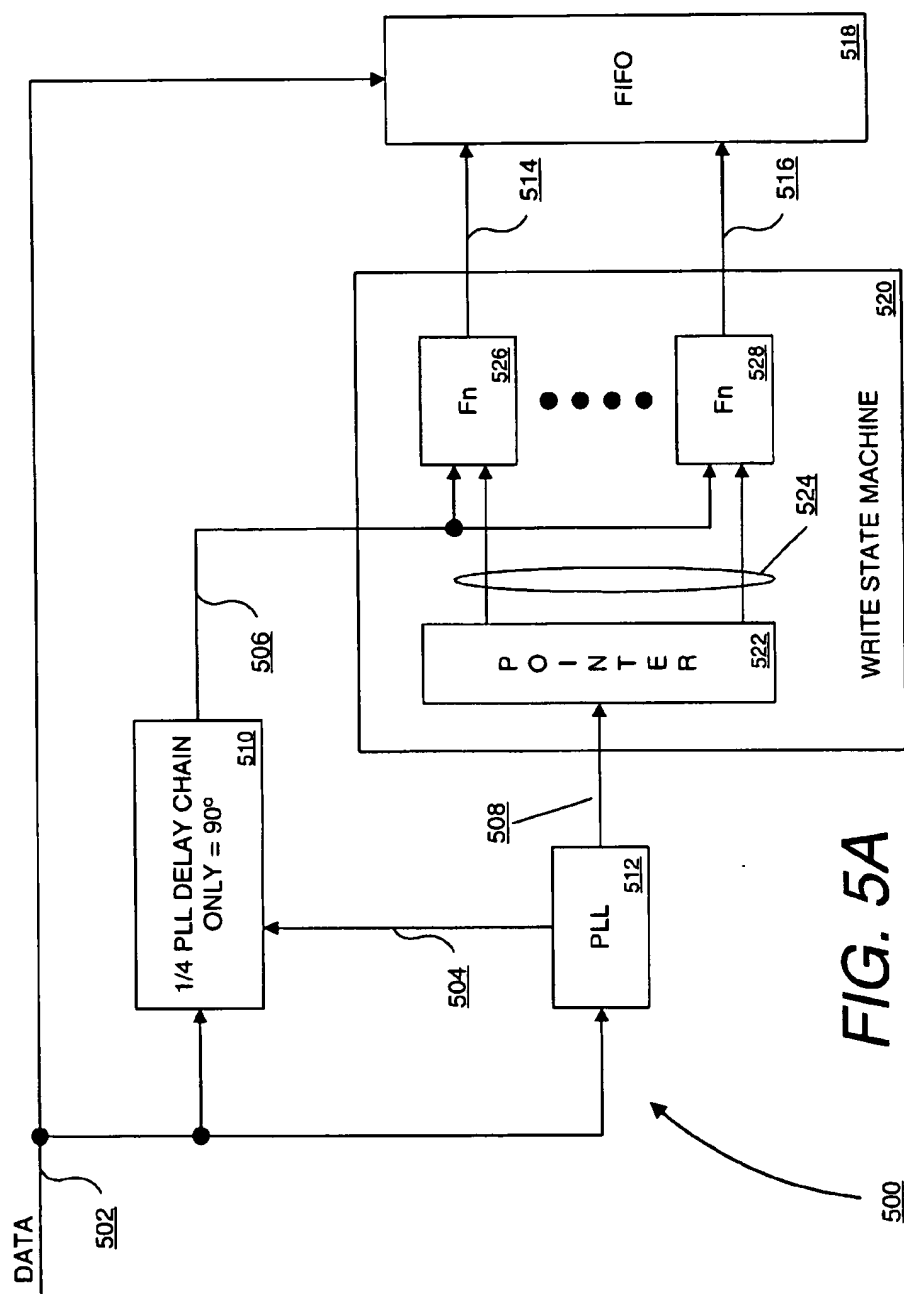
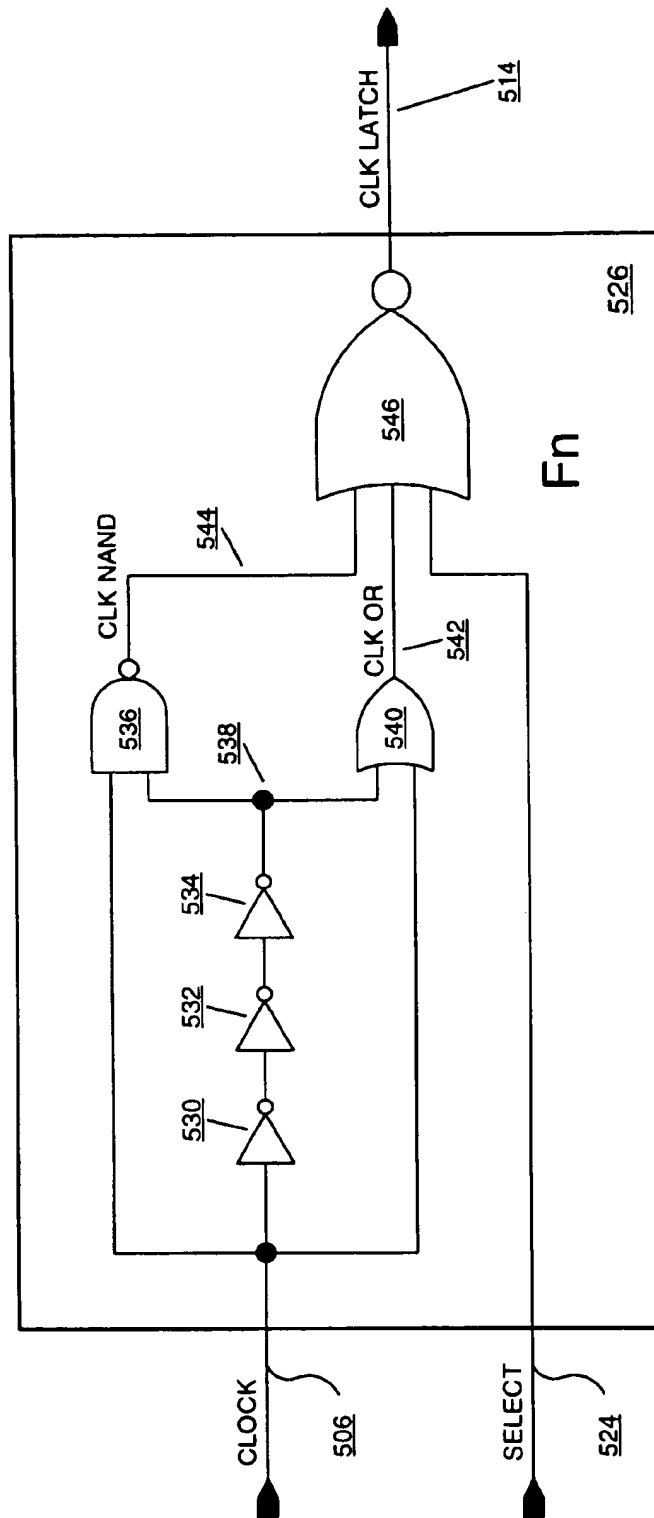


FIG. 4

**FIG. 5A**

**FIG. 5B**

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# SYSTEM FOR PROTECTING STROBE GLITCHES BY SEPARATING A STROBE SIGNAL INTO POINTER PATH AND TIMING PATH, FILTERING GLITCHES FROM SIGNALS ON POINTER PATH THEREOF

## FIELD OF THE INVENTION

The present invention relates generally to the field of signal transfer between components, and more specifically to a strobe glitch protection mechanism for a source synchronous I/O link.

## BACKGROUND OF THE INVENTION

One limitation on the throughput of a computer or other processing system is the interface between integrated circuits and/or other components in the system. Interface circuits often provide input/output (I/O) links for data transfers between components. Improved data transfer circuitry may allow faster and more efficient signaling between various components.

I/O links between components and systems often use data, reference voltage and strobe lines. The reference voltage provides a threshold which allows a signal to be qualified as low or high state, whereas the strobe provides the timing reference i.e. the position of the data bit in a time sequence. The strobe signal functions as a transfer clock. In some data transfer communications, glitches can occur in these signals. A glitch is generally defined as an undesired transition or bounce in a signal. Glitches destroy the integrity of signals on a line. Sources of glitches can include interference, cross talk, ground bounce, mechanical vibrations, etc. Data glitches can cause corruption of data if the glitch occurs at the sampling time at the receiver. Data error checking techniques such as parity or error-correcting code (ECC) can detect and possibly correct an error. However, any glitches in the strobe signal can alter the state machine and disturb the timing context, therefore corrupting future data. Therefore, a strobe glitch can have a catastrophic effect on the I/O link.

There are two types of strobe failures of concern. The first type is an analog glitch or noise that is long enough to cause errant internal strobe behavior, but does not manifest as a double pulse. This type of behavior can be difficult to detect. This error can amount to a slower signal transition edge or a moved edge, but not a full transition. During such a failure, the phase of the strobe with respect to the incoming data could be lost. The second type of strobe failure involves signal noise that creates a double pulse that may be mistakenly counted at the receiver. A double pulse can cause the logic in a state machine to erroneously increment to the next state.

One existing glitch protection scheme can only protect against glitches during master changeover scenarios. Another existing scheme can only detect an error and then flag the error during a break in bus activity. Other glitch protection schemes have used a phase locked loop (PLL) to filter strobe signals. However, a PLL also filters out data and strobe cycle to cycle timing jitters, leading to undesired loss of timing margin.

FIG. 1 illustrates a block diagram of a typical prior art source synchronous strobe and data circuit 100 at a receiver. The circuit 100 receives a data signal 102 and a strobe signal 103 that have been sent from an external data transfer source. Data 102 is connected to a latch mechanism. The latch mechanism in this example is a set of first in/first out

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(FIFO) latches 118. Strobe 103 is connected to a delayed lock loop (DLL) 112. The DLL 112 is a chain of delay element that delays the propagation of strobe 103 to node 108 by a desired amount (usually 90°). The delayed version of strobe at node 108 is coupled to a write state machine (WSM) 120 at pointer 122 and latch enable logic 126, 128. Pointer 122 generates a plurality of latch select signals 124 based on transitions on strobe 103. Latch enables 114, 116 to the FIFO 118 are generated from latch enable logic 126, 128. For this example, latch selects 124 are logically ANDed together with delayed strobe 108 at AND gates 126, 128.

The DLL 112 rotates STROBE 103 to a 90° position. This 90° phase shift allows the strobe signal to center the data window. However, the DLL 112 only performs a rotation and delays STROBE 103. If STROBE 103 is noisy or has glitches, the noise and glitches are simply rotated 90° and propagated out to the WSM 120.

This example circuit at the receiver end of the data transfer uses a strobe having a 90° rotation to advance the write pointer and latch incoming data. In other circuits, the strobe can be set at a 90° position at the driver end. But in either case, the noise and degraded signal quality can cause strobe glitches. It may be especially advantageous to identify options for strobe glitch protection and detection.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitations in the figures of the accompanying drawings, in which like references indicate similar elements, and in which:

FIG. 1 illustrates a block diagram of a typical prior art source synchronous strobe and data circuit at a receiver;

FIG. 2A illustrates one embodiment of a system employing a strobe glitch protection mechanism;

FIG. 2B illustrates one embodiment of a parallel I/O link between two components;

FIG. 2C illustrates one embodiment of a serial I/O link between two components;

FIG. 3A illustrates one embodiment of a single ended source synchronous strobe and data circuit having a modified strobe path at the receiver end of a parallel I/O link;

FIG. 3B illustrates one embodiment of strobe glitch mechanism in the modified strobe path of FIG. 3A;

FIG. 3C illustrates another embodiment of the modified strobe path of FIG. 3A including a glitch filtering mechanism;

FIG. 3D illustrates a flow chart of a method for strobe glitch protection for one embodiment;

FIG. 4 illustrates one embodiment of a single ended source synchronous strobe and data circuit including a differential VCO at the receiver end of a parallel I/O link;

FIG. 5A illustrates one embodiment of a data circuit at the receiver end of a serial I/O link; and

FIG. 5B illustrates one embodiment of the latch enable mechanism of FIG. 5A.

## DETAILED DESCRIPTION

A strobe glitch protection mechanism for a source synchronous I/O link is disclosed. The described strobe and data circuits are used to transfer data between integrated circuits, but are not so limited. Although the following embodiments are described with reference to processors, other embodiments are applicable to other integrated circuits or logic devices. The same techniques and teachings of the present

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invention can easily be applied to other types of circuits or semiconductor devices that use a synchronous I/O link.

In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. One of ordinary skill in the art, however, will appreciate that these specific details are not necessary in order to practice the present invention. In other instances, well known electrical structures and circuits have not been set forth in particular detail in order to not necessarily obscure the present invention.

During a data transfer, a source device sends data via a link to a receiver device. Typical devices can include items ranging from integrated circuit components to systems. When a source sends data to a receiver, a strobe or clock is also sent to the receiver. However, the exact arrival of a signal at the receiver and its signal quality can vary due to factors such as line discontinuities, parasitic capacitance & inductance, propagation delay, etc. The receiver has to know exactly when a signal is arriving and how to react.

When data arrives at the receiver, the data generally needs to be stored or latched away. Furthermore, if bits of data are being constantly transmitted and received, the receiver has to keep track of what bits are coming in and how to shift the data bits in the correct order. Logic, such as a write state machine, can place the bits in time sequence using the strobe as they arrive at the receiver.

Preserving the precise order of the data bits is critical. A strobe signal from the receiver often assists in this process. The strobe can serve two functions. First, a strobe signal can be used to capture data into a latch. Second, a strobe can help to place the bits in a proper sequence. For example, a receiving device can have a set of latches that behave like a cyclic buffer. Every time the strobe signal toggles, the receiver latches a data bit into a latch and advances a pointer to the next latch. The pointer advancement prevents the incoming bit from overwriting the stored data. Meanwhile, other logic in the receiving device can be reading out data from the previously written latches. By the time the last latch is filled, the first latch has been freed up and ready for new data. The pointer can wrap around and the latches are rewritten.

In source synchronous input/output (I/O) signaling, a precisely known data and strobe timing relationship is used to capture data at a receiver. Maintaining the integrity of the strobe signal and the write pointer is of great importance. The strobe edge is used to time the data and also to advance the state machine. Any glitches in the strobe can result in the incorrect advancement of the write pointer and also incorrect data capture. Incorrect data capture can be detected by using parity or ECC or CRC checks. However, an incorrect write pointer can lead to errors in subsequent data transfers and ultimately system failure. Strobe glitch issues can also be present in point to point links. Two types of problems can have an impact on data transfer. The first involves having extra pulses on the strobe signal. A second problem involves missing pulses on the strobe. In order to prevent strobe glitches, some circuit designers have implemented strobe glitch protection circuits into their components and systems.

A strobe glitch protection circuit can filter out the glitches and prevent the state machine from advancing states erroneously. Furthermore, the circuit can be configured to allow the data timing information to propagate through for proper data capture. These actions can be achieved by splitting the incoming strobe signal into two separate paths. One timing strobe path can retain the timing information and jitter. The other strobe path can be filtered to obtain a clean pointer strobe signal.

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Embodiments of the present invention allow the write pointers to operate on clean strobes. Thus, accurate write state machine information can be maintained. Furthermore, the system reliability of a system or a component implementing an embodiment of the present scheme may not be limited by write pointer accuracy. This strobe glitch protection mechanism also provides an accurate cycle by cycle tracking between the data and strobe signals. Signal timing in the critical timing path is preserved as the path is kept free of additional circuit elements.

Depending on the implementation, alternative embodiments of the present mechanism can require fewer additional circuit elements than other glitch schemes. One method of present invention can also be adapted for use in a self clocked serial I/O link where no explicit strobing clocks are available.

Referring now to FIG. 2A, a computer system 200 is shown. System 200 includes a component, such as a processor, employing a strobe glitch protection mechanism in accordance with the present invention, such as in the embodiment described herein. System 200 is representative of processing systems based on the PENTIUM®, PENTIUM® Pro, PENTIUM® II, PENTIUM® III microprocessors available from Intel Corporation of Santa Clara, Calif., although other systems (including PCs having other microprocessors, engineering workstations, set-top boxes and the like) may also be used. Thus, the present invention is not limited to any specific combination of hardware circuitry and software.

FIG. 2A is a block diagram of one embodiment of a system 200. The computer system 200 includes a processor 202 that processes data signals. FIG. 2A shows an example of an embodiment of the present invention implemented in a single processor system 200. However, it is understood that other embodiments may alternatively be implemented as systems having multiple processors. Processor 202 is coupled to a processor bus 210 that transmits data signals between processor 202 and other components in the system 200. The elements of system 200 perform their conventional functions well known in the art.

System 200 includes a memory 220. A cache memory 204 can reside inside processor 202 that stores data signals stored in memory 220. Alternatively, in another embodiment, the cache memory may reside external to the processor.

A strobe glitch protection mechanism 206 also resides in processor 202. Alternate embodiments of a strobe glitch protection mechanism 206 can also be used in microcontrollers, embedded processors, graphics devices, DSPs, and other types of logic circuits.

A system logic chip 216 is coupled to the processor bus 210 and memory 220. The processor 202 communicates to a memory controller hub (MCH) 216 via a processor bus 210. The MCH 216 directs data signals between processor 202, memory 220, and other components in the system 200 and bridges the data signals between processor bus 210, memory 220, and system I/O 222. The graphics card 212 is coupled to the MCH 216 through an Accelerated Graphics Port (AGP) interconnect 214.

System 200 uses a proprietary hub interface bus 222 to couple the MCH 216 to the I/O controller hub (ICH) 230. The ICH 230 provides direct connections to I/O devices such as a firmware hub (BIOS) 228, data storage 224, a serial expansion port such as Universal Serial Bus (USB), and a network controller 234.

The present enhancement is not limited to computer systems. Alternative embodiments of the present invention

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can be used in other devices such as, for example, handheld devices and embedded applications. Some examples of handheld devices include cellular phones, Internet Protocol devices, digital cameras, personal digital assistants (PDAs), and handheld PCs. Embedded applications can include a microcontroller, a digital signal processor (DSP), system on a chip, network computers (NetPC), set-top boxes, network hubs, wide area network (WAN) switches, or any other system which uses a latch type mechanism for other embodiments.

FIG. 2B illustrates one embodiment of a parallel I/O link between two components 240, 250. This example shows component A 240 communicating with component B 250 via a parallel I/O link. Parallel here refers to the use of separate signals for data 260 and strobe 262, and not the presence of multiple data lines in the link. During a data transfer, data 260 and strobe 262 are both driven from A 240 to B 250. Strobe 262 can be used to notify the receiver as to when data is available.

Component A 240 comprises a data source 242 and a strobe source 246. Data source 242 provides a data signal to an output driver 244, which in turn drives data 260 from component A 240 to component B 250. Strobe source 246 provides a strobe signal to an output driver 248, which in turn drives strobe 262 from A 240 to B 250.

Component B 250 comprises a data receiver 252 and a strobe receiver 256. Data signal 260 is received at input driver 254, which in turn provides the data to data receiver 252. Data receiver 252 may be a latch type mechanism. Strobe 262 is received at input driver 258 and propagated to strobe receiver 256. Strobe receiver 256 may be a write state machine.

FIG. 2C illustrates one embodiment of a serial I/O link between two components. This example shows component A 270 communicating with component B 278 via a serial I/O link. Serial here refers to the use of only a data signal and the absence of a strobe signal. During a data transfer, data 276 is driven from A 270 to B 278. Data 276 can include an embedded clock to notify the receiver as to when data is available.

Component A 270 comprises a data source 272. Data source 272 provides a data signal to an output driver 274, which drives data 276 from A 270 to B 278. Component B 278 comprises a data receiver 280. Data signal 276 is received at input driver 282, which provides the data to data receiver 280. Data receiver 278 may be a logic circuit that can generate a strobe from the embedded clock in data and latch the data.

FIG. 3A illustrates one embodiment of a single ended source synchronous strobe and data circuit 300 having a modified strobe path at the receiver end of a parallel I/O link. This circuit 300 receives a data signal DATA 302 and a strobe signal STROBE 303 from a data transfer source. DATA 302 is coupled to a set of FIFO latches 318. For alternative embodiments, other types of latch mechanisms can be used. STROBE 303 is coupled to a write state machine (WSM) 320 through a modified strobe path.

The modified strobe path 311 of the embodiment described here provides a first strobe 306 derived from a delay element 310 and a PLL filtered strobe 308 to the WSM 320. For this example, both the first strobe 306 and the PLL filter strobe 308 are rotated 90° relative to STROBE 303. The 90° rotation on the strobe signals centers the data window for latching. By splitting STROBE 303 into two separate signals, this scheme can provide a robust strobe 308 to the WSM 320 and also allow for tight data/strobe match-

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ing in the timing path. The timing path of FIG. 3A traces from the delay chain 310, along node 306, and through the latch enable logic 326, 328 to the FIFO latches 318.

The modified strobe path comprises a strobe glitch protection mechanism 311 that is coupled to STROBE 303. Strobe glitch protection mechanism 311 provides two versions of a delayed strobe 306, 308 to WSM 320. For this embodiment, the strobe glitch protection mechanism 311 comprises of a delay chain 310 and a phase locked loop (PLL) 312. The delay chain 310 is a ¼ PLL delay chain having a phase shift of 90° (or the desired rotation). The delay chain 310 generates a first delayed strobe 306 by shifting STROBE 303 by 90° as STROBE 303 passes through. Delayed strobe 306, also known as the timing strobe, is unfiltered relative to STROBE 303 such that cycle to cycle jitter is preserved to match DATA 302. Timing strobe causes the latching action to occur in the latches 318. By keeping the timing strobe in phase with DATA 302, timing loss and noise margins may be reduced. Hence, the timing paths of the DATA 302 and timing strobe are preserved from the output latch or driving pad of the sender over to the inbound latch of the receiver.

PLL 312 of this embodiment includes a voltage controlled oscillator such as a large inverter chain or a ring oscillator. The oscillator provides an oscillating signal based on the voltage level of a control signal. The oscillator can be controlled to speed up or slow down as desired. The oscillator is inputted a frequency at which to function. A phase detector attempts to lock the input and output signals of the oscillator.

The PLL 312 takes STROBE 303 and generates a second delayed strobe 308, pointer strobe. This second delayed strobe 308 is PLL filtered and rotated 90° with respect to STROBE 303. Pointer strobe 308 causes the WSM 320 to point at the latch to store DATA 302. Glitches are not desirable on the pointer strobe 308 because an incorrect pointer strobe 308 can lead to latching data in the wrong sequence. Noise and glitches can occur on signal lines due to transmission line reflections, mismatches, ground bounce, etc. PLL 312 also provides a control signal 304 to delay chain 310. Control signal 304 can cause the delay in the delay chain 310 to vary as needed. The shared control 304 of some embodiments can include analog voltages or digital bits.

If an extra pulse is seen on STROBE 303, pointer strobe 308 is still properly supplied a pulse from the oscillator. The PLL 312 tries to speed up the oscillator to catch up with the extra strobe pulse. However, the loop time constant is extremely large and the acceleration of the oscillator is converted to jitter instead. Similarly, when a pulse is missing on STROBE 303, pointer strobe 308 is still properly supplied a pulse from the oscillator. The PLL 312 tries to slow the oscillator to make up for the missing pulse. However, the loop time constant is extremely large and the deceleration of the oscillator is converted to opposite jitter. In either situation, the strobe glitch protection mechanism 311 is able to recover from the problem with STROBE 303. The glitches are converted to jitter and do not incorrectly advance or miss advancing the latch pointers.

The circuit 300 of the present embodiment is designed to latch data on the edge transition of a strobe pulse. The actual width of the strobe pulse is as important here. However, the strobe pulse should be reasonably close to the center of the timing window in order to maximize timing margins.

For this embodiment, an accurate strobe rotation path is provided by inserting a delay element path through delay

chain 310 in parallel with PLL 312. Control elements in PLL 312 such as a delay element, control voltages, or control bits, can be shared with the delay chain 310 as with control signal 304. Cycle by cycle jitter tracking of the DATA 302 and STROBE 303 signals is also available.

The PLL 312 in the modified strobe path 311 of this embodiment filters out any occasional glitches in the strobe signal 303. The glitch is converted into additional jitter in the PLL 312 instead of being propagated as an invalid transition to WSM 320. Hence, the WSM 320 should get a clean strobe signal 308 and be able to maintain accurate state information.

The PLL 312 of one embodiment can use the same low pass filtering (LPF) capacitor as that of a DLL 112 in FIG. 1. An embodiment of the present strobe glitch mechanism may be implemented so that there are only small differences in performance characteristics such as area and power capture range between the DLL 112 and the PLL 312 solutions.

The first delayed strobe 306 is coupled to the latch enable logic 326, 328 in the WSM 320. The second delayed strobe 308 coupled to the pointer logic 322, which generates a plurality of latch select signals 324. Pointer logic 322 enables only one of the latch enable logic 326, 328. Latch select signals 324 are coupled to the latch enable logic 326, 328. Latch enable logic 326, 328 of this embodiment logically and together the first delayed strobe signal 306 and latch select signals 324 to generate a latch enable signal 314, 316. When the timing strobe 306 transitions, the selected latch enable logic will generate a pulse to the latches 318 to perform the latching action. Each one of these latch enable signals 314, 316 are used to sequentially activate a corresponding latch 318 to receive and store DATA 302. DATA 302 is not limited to a single data line. For alternative embodiments, the larger number of data lines may be used.

FIG. 3B illustrates one embodiment of the strobe glitch mechanism 311 in the modified strobe path of FIG. 3A. This glitch strobe mechanism 311 comprises a delayed chain 310 and a PLL 312. STROBE 303 is connected to both the delay chain 310 and the PLL 312. The exemplary strobe glitch mechanism 311 of FIG. 3B includes two different strobe paths 306, 308.

Delay chain 310 of this embodiment is a  $\frac{1}{4}$  PLL delay chain proving a  $90^\circ$  phase shift for STROBE 303. STROBE 303 is connected to the input of inverter 330. Delay chain 310 comprises an inverter 330 with a delay of  $\tau$  chained to a fast inverter 332 with a delay of  $\tau'$ . Delay  $\tau$  of this embodiment is much larger than delay  $\tau'$ . Inverter 330 is controlled with a control signal 304 that is generated from a phase detector and filter circuit 334 in the PLL 312. Control signal 304 can alter the transition speed of inverter 330. TIMING STROBE 306 is outputted from fast inverter 332. TIMING STROBE 306 of this embodiment is not filtered and retains the jittering characteristics of STROBE 303. Thus TIMING STROBE 306 can track the jittering of DATA 302.

STROBE 303 is connected to a phase detector and filter circuit 334. PLL 312 of this embodiment comprises a phase detector and filter circuit 334 and an oscillator inverter chain. Since a voltage controlled oscillator requires an odd number of inversions, extra inverter stages 346, 348, 350 were added to the oscillator of this embodiment. This inverter chain comprises of four inverters 338, 340, 342, 344 with delay  $\tau$  chained to three fast inverters 346, 348, 350 with delay  $\tau'$ . The output 336 of the inverter chain from inverter 344 is fed into the phase detector and filter circuit

334. A control signal 304 is generated based on the sampled signal 336 and STROBE 303. The transition rate of inverters 338, 340, 342, 344 can be modified by control signal 304 to speed up or slow down.

5 POINTER STROBE 308 is tapped from the inverter chain between the first fast inverter 346 and the second inverter 340. Because delay  $\tau$  of this embodiment is much greater than  $\tau'$ , the phase shifts is predominately due to inverters 338, 340, 342, 344. Each of the inverters 338, 340, 342, 344 provide a phase shift of approximately  $90^\circ$ . The signal at node 308 is shifted approximately  $90^\circ$  from STROBE 303. The signal at node 336 has an offset of  $0^\circ$  degrees from STROBE 303. The signal between the second inverter 340 and the second fast inverter 348 has an offset of approximately  $180^\circ$  from STROBE 303. The signal between the third inverter 342 and the third fast inverter 350 has an offset of approximately  $270^\circ$  from STROBE 303. The phase shift of the signal between the fourth inverter 344 and STROBE 303 is approximately  $360^\circ$ . The fast inverters 346, 348, 350 invert the signal, but cause minimal phase shifts. Thus the error of the signal position of the transitions in the oscillator with respect to STROBE 303 is minimal. For this embodiment, POINTER STROBE 308 is a filtered and  $90^\circ$  rotated version of STROBE 303.

25 FIG. 3C illustrates another embodiment of the modified strobe path of FIG. 3A including a glitch filtering mechanism 360. STROBE 303 is coupled the input terminal of an inverter 355. Inverter 355 provides a  $180^\circ$  phase shifted version of STROBE 303 at its output terminal. For alternative embodiments, this shift may be performed at the data sender, making this inverter 355 unnecessary. The output terminal of inverter 355 is TIMING STROBE 306. This glitch filtering circuit 360 filters STROBE 303 for the pointer path.

35 TIMING STROBE 306 is also coupled to the glitch filtering mechanism 360. The logic of this circuit 360 can be designed to catch and filter out certain types of glitches in the input signal, TIMING STROBE 306 in this example. This mechanism 360 includes an inverter delay chain 361 having a total delay of  $\tau_D$ . The number of inverters in the delay chain 361 can be increased and decreased to obtain the desired delay. For this embodiment, the inverter chain 361 propagates TIMING STROBE 306 through three inverters 362, 364, 366. The output of the final inverter 366 of inverter chain 361 is connected to a second terminal of nand gate 368 and a second terminal of nor gate 376. TIMING STROBE 306 is connected to a first terminal of nand gate 368 and a first terminal of nor gate 376.

50 Logic gates 372, 380, 384 are connected together to form an R-S type latch mechanism. Node 370 can be viewed as SET#, node 378 as RESET, node 382 as RESET#, node 374 as Q, and node 386 as Q#. The output terminal 370 of nand gate 368 is connected to a first input of nand gate 372. The output terminal 374 of nand gate 372 is fed to a first input terminal of nand gate 384. The output terminal 378 of nor gate 376 is connected to the input terminal of inverter 380, whose output terminal 382 is connected to a second input terminal of nand gate 384. The output terminal 386 of nand gate 384 is fed to a second input terminal of nand gate 372. The output terminal 386 of nand gate 384 is also connected to the input terminal of inverter 388, whose output terminal is connected to the input of output driver 390. The signal at the output terminal of driver 390 is POINTER STROBE 308.

65 Glitch filtering circuit 360 takes an incoming signal, node 306 in this example, and filters out certain types of glitches.



The path through delay chain 361 has a delay of  $\tau_D$ . The circuit 360 of this embodiment filters out transitions on the incoming signal that occur within a window of width D provided that  $\tau_D$  is greater than D. Time D is the time duration of the glitch or transitions. If the incoming signal 5 has a certain time D, then the circuit 360 of this embodiment can filter out the glitches or movements if D is less than  $\tau_D$ . The delay may be stabilized across process voltage and temperature variations using a compensated delay chain 10 such as used in a Voltage Controlled Oscillator.

It should be noted that the filtered pointer strobe is delayed by  $\tau_D$ , that may be acceptable in slower interfaces. For fast interfaces, the delay in the pointer strobe path must be matched by the timing strobe path delay.

FIG. 3D illustrates a flow chart of a method for strobe glitch protection for one embodiment. For this embodiment, a transfer clock is separated into a pointer path and a timing path at step 392. The pointer path comprises a pointer strobe and the timing path comprises a timing strobe. At step 394, 20 glitches are filtered from the pointer path. The pointer path and timing path are coupled at step 396 to generate latch enable signals to latch data bits.

For alternative embodiments, such as in a serial link, the method for strobe glitch protection will be different from FIG. 3D. In a serial I/O link, a data input having a plurality of signal transitions is received. The data input comprises of data and an embedded clock. A clock signal is extracted from the data input. A timing strobe and pointer strobe are generated. A latch enable signal is in turn generated from the timing strobe and pointer strobe. The latch enable signal is used to latch data from the data input.

FIG. 4 illustrates another embodiment of a single ended source synchronous strobe and data circuit 400 including a differential voltage controlled oscillator (VCO) 415 at the receiver end of a parallel I/O link. This circuit 400 takes 35 single ended inputs, such as DATA 402 and STROBE 403, and converts the signals into differential signals. Hence this embodiment can be used in a singled ended implementation.

DATA signal 402 comes into the input of a single ended to differential converter 405. Similarly, STROBE signal 403 is connected to the input of another single ended to differential converter 411. Control signal CNTL 401 is connected to the differential converters 405, 411 to adjust and set the delay (usually least). The signal paths and differential converters 405, 411 on DATA 402 and STROBE 403 are 45 matched in order to maintain the transition and timing relationships of the signals. The inverted version of DATA 402 at that output terminal 407 of differential converter 405 is connected to the FIFO latches 418.

The two outputs (normal 419 and inverted 421) of the strobe differential converter 411 are connected to a phase detector and filter 413 and a third differential converter 417. The third differential converter 417 provides a 90° shifted 55 inverted output 406 of the signals 419, 421. This inverted output SHIFT STROBE 406 is coupled to latch enable logic 426, 428 in the WSM 420.

The differential VCO 415 of this example comprises of four differential converters 430, 432, 434, 436 chained 60 together. The outputs 438, 440 of the final stage 436 are fed back to the input terminals of the first stage 430 and also to the phase detector and filter 413. The phase detector and filter circuit samples the outputs 419, 421 of the strobe differential converter and the outputs 438, 440 of the last stage 436 in the VCO 415, and generates a control signal 404. Control signal 404 is connected to the differential

converters 430, 432, 434, 436 of the VCO 415 and the strobe differential converter 417.

For this embodiment, the differential VCO is set for accurate 90° delays. The four differential converters 430, 432, 434, 436 in the VCO 415 each provide a 90° shift in the signal. POINTER STROBE 408 is tapped off at the 90° point between the first 430 and second 432 converters. POINTER STROBE 403 is coupled from the VCO 415 to pointer logic 422 in the WSM 420. Pointer logic 422 generates a plurality of latch select signals coupled to latch enable logic 426, 428. Latch enable logic 426, 428 logically 15 and together the TIMING STROBE 406 and latch select signals to generate latch enable signals 414, 416. Each one of these latch enable signals 414, 416 are used to sequentially activate a corresponding latch 418 to receive and store the shifted version 407 of DATA 402. Further it must be noted that the write state machine and the timing path and the FIFO can be maintained differential after the single ended to differential conversion. Also the circuit shown in FIG. 4 is easily adapted to differential data and strobe signals. The single ended to differential stages 405 and 411 are replaced by differential receivers.

Not all data transfers or communications are performed over parallel I/O links having separate data and strobe lines. A serial I/O link may also be used. Serial links can be 25 cheaper than parallel links since only one signal line is needed, and they can be faster as there is no interconnect induced skew between strobe and data. For instance, a transmission medium such as a cable link is expensive. Minimizing the number of wires needed can reduce costs.

A serial link does not have an explicit strobing clock. Serial I/O links with an embedded clock are also used to transfer data. In serial links, the latching of the data occurs using a recovered clock from the data stream. The clock recovery employs a special PLL which uses the data transitions to act as the reference. This PLL effectively isolates the data and clock jitter tracking on a cycle by cycle basis.

FIG. 5A illustrates one embodiment of a data circuit 500 at the receiver end of a serial I/O link. This circuit 500 receives a data signal DATA 502 from a data transfer source. DATA 502 is coupled to a set of FIFO latches 518, a PLL delay chain 510, and a PLL 512. This serial I/O link does not include a strobe signal. The latching edge to capture DATA 502 in the FIFO latches 518 needs to be generated from DATA 502 itself. For this embodiment, the latching clock 506 needs to include the pointer position and trigger edge. The trigger edge can be a low to high transition or a high to low transition depending on the data values. A clock can be created by including a edge to pulse converter circuit in delay chain 510 or elsewhere along the critical timing path. The critical timing path of this example traces from the delay chain 510, along clock signal 506, through latch enable logic 526, 528, and latch enables 514, 516 to the latches 518.

The PLL delay chain 510 of this embodiment provides a phase shift of 900 to DATA 502 and generates a clock signal 506 as a delayed version of DATA 502. The clock signal 506 is coupled to latch enable logic 526, 528 in the WSM 520. The latch enable logic of this embodiment is a logic block 60 Fn 526, 528 able to generate select signals 514, 516 for a serial link. The delay chain 510 of this embodiment also preserves timing jitters in DATA 502 and thus maintaining the clocking relationship between DATA 502 and clock signal 506. Timing margin is also improved in the data latching operations.

The PLL 512 of this embodiment is designed to use the intermittent signal transitions edges of DATA 502 to latch.

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The PLL 512 transforms faulty edges into a jitter term. The PLL 512 takes DATA 502 and generates a POINTER STROBE signal 508 to pointer logic in the WSM 520. PLL 512 also provides a control signal 504 to delay chain 510. Control signal 504 can cause the delay in the delay chain 510 to vary as needed. The pointer logic 522 generates a plurality of latch select signals 524, which are coupled to Fn 526, 528. Fn 526, 528 uses clock signal 506 and latch select signals 524 to generate latch enable signals 514, 516. Each one of these latch enable signals 514, 516 are used to sequentially activate a corresponding latch 518 to receive and store DATA 502. If there is no data edge, such as when two consecutive data bits are the same level, then the pointer strobe 508 is toggled and latch select signals 524 advanced appropriately.

FIG. 5B illustrates one embodiment of the latch enable mechanism Fn 526 of FIG. 5A. Input signals CLOCK 506 and SELECT 524 are coupled to Fn 526. CLOCK 506 is connected to a first terminal of nand gate 536, to a first terminal of or gate 540, and to the input terminal of inverter 530. Three inverters 530, 532, 534 for a delay chain. A delayed version 538 of CLOCK 506 is propagated from the output terminal of inverter 534 to a second input terminal of nand gate 536 and to a second input terminal of or gate 540.

CLOCK signal 506 and the delayed CLOCK 538 signal are nanded together to generate CLK NAND 544. CLOCK signal 506 and the delayed CLOCK 538 signal are ored together to generate CLK OR 542. The output signal CLK NAND 544 from nand gate 536 is connected to an input terminal of nor gate 546. Similarly, the output signal CLK OR 542 of or gate 540 is connected to as second input terminal of nor gate 546. SELECT 524 is connected to a third input terminal of nor gate 546. The output of the three input nor gate 546, and Fn 526, is CLK LATCH 514. CLK LATCH 514 can be activated to enable a latch to capture data.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereof without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A method comprising:

separating a transfer clock having a plurality of transfer clock edges into a pointer path and a timing path, wherein said pointer path and said timing path have dissimilar timing;

filtering glitches from signals on said pointer path and allowing certain glitches from said transfer clock to appear on signals on said timing path; and

coupling said pointer path and said timing path to generate latch enable signals to latch data bits.

2. The method of claim 1 wherein said timing path comprises a timing strobe, said timing strobe retaining jittering of said transfer clock.

3. The method of claim 1 wherein said pointer path comprises a pointer strobe.

4. The method of claim 3 wherein said pointer strobe activates latch enable logic.

5. The method of claim 1 further comprising generating a clock signal for said pointer path.

6. The method of claim 1 further comprising delaying propagation of said transfer clock to said timing path.

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7. An apparatus comprising:

a strobe glitch protection mechanism configured to receive a strobe signal, said glitch protection mechanism further configured to provide a timing strobe and a pointer strobe, said timing strobe to include timing information from said strobe signal, and said pointer strobe to be filtered of one or more glitch on said strobe signal; and

a state machine coupled to said strobe glitch protection mechanism, said state machine configured to receive said timing strobe and said pointer strobe, and to generate a latch enable signal based on said timing strobe and said pointer strobe.

8. The apparatus of claim 7 wherein said glitch protection mechanism comprises a phased locked loop to generate a pointer strobe.

9. The apparatus of claim 7 wherein said glitch protection mechanism comprises a delay mechanism to generate a timing strobe.

10. The apparatus of claim 7 wherein said glitch protection mechanism comprises a glitch filter mechanism to remove glitches having a duration less than a set time limit on said strobe signal.

11. The apparatus of claim 7 wherein said pointer strobe is rotated 90° relative to said strobe signal.

12. The apparatus of claim 7 wherein said timing strobe is rotated 90° relative to said strobe signal and retains jittering of said strobe signal.

13. The apparatus of claim 7 wherein said strobe glitch mechanism splits said strobe signal into a timing path and a pointer path.

14. The apparatus of claim 7 further comprising a latch mechanism coupled to said state machine.

15. The apparatus of claim 7 wherein said latch enable signal is used latch data bits.

16. An integrated circuit device comprising:

a data input configured to receive data bits;

a strobe input configured to receive a strobe signal;

a circuit coupled to said data input and said strobe input, said circuit to configured to receive data from an I/O link, said circuit comprising:

a strobe glitch protection mechanism to receive a strobe signal, said glitch protection mechanism configured to provide a timing strobe and a pointer strobe, said timing strobe including timing information from said strobe signal, and said pointer strobe filtered of one or more glitch appearing on said strobe signal;

a state machine coupled to said strobe glitch protection mechanism, said state machine configured to receive said timing strobe and said pointer strobe, and to generate a latch enable signal based on said timing strobe and said pointer strobe; and

a latch mechanism coupled to said write state machine, said latch mechanism configured to receive a plurality of data bits and said latch enable signal, said latch mechanism to latch said data bits in accordance with said latch enable signal.

17. The integrated circuit device of claim 16 wherein said integrated circuit device is a processor.

18. The integrated circuit device of claim 16 wherein said integrated circuit device is a firmware hub.

19. The integrated circuit device of claim 16 wherein said integrated circuit device is a memory device.

20. A system comprising:

a system bus, said bus configured to propagate data bits and a clock signal;

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an I/O interface coupled to said system bus;  
 a component coupled to said system bus, said component to receive data from an I/O link during a data transfer, said component comprising:  
 a strobe glitch protection mechanism configured to receive a strobe signal, said glitch protection mechanism further configured to provide a timing strobe and a pointer strobe, said timing strobe to include timing information from said strobe signal, and said pointer strobe to be filtered of one or more type of glitch on said strobe signal;  
 a state machine coupled to said strobe glitch protection mechanism, said state machine configured to receive said timing strobe and said pointer strobe, and to generate a latch enable signal based on said timing strobe and said pointer strobe;  
 a latch mechanism coupled to said write state machine, said latch mechanism configured to receive a plurality of data bits and said latch enable signal, said latch mechanism to latch said data bits in accordance with said latch enable signal.

21. The system of claim 20 wherein said timing strobe retains jittering of said strobe signal.

22. The system of claim 20 wherein glitches are filtered from said pointer strobe.

23. The system of claim 20 wherein said strobe glitch mechanism splits said strobe signal into a timing path and a pointer path.

24. The system of claim 20 wherein said I/O interface is coupled to data transfer source.

25. A method comprising:  
 receiving a data input having a plurality of signal transitions, said data input comprising data and an embedded clock;  
 extracting a clock signal from said data input and generating a timing strobe and a pointer strobe, said timing strobe to include timing information from said strobe signal, and said pointer strobe to be filtered of at least one type of glitch on said strobe signal;

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generating a latch enable signal from said timing strobe and said pointer strobe; and  
 using said latch enable signal to latch said data from said data input.

26. The method of claim 25 wherein said timing strobe retains jitters of said data input.

27. The method of claim 25 wherein said timing strobe is a delayed version of said data input.

28. The method of claim 25 wherein said pointer strobe controls activation of latching.

29. A method comprising:  
 separating a strobe signal into a pointer strobe on a pointer path and a timing strobe on a timing path, said pointer strobe filtered of one or more strobe glitches that appear on said strobe signal, said timing strobe unfiltered of said strobe glitches and retaining timing information and jitter from said strobe signal;  
 generating a select signal in response to said pointer strobe, said select signal to select one of a plurality of data latches;  
 generating a latch enable signal in response to said timing strobe for said selected data latch, said latch enable signal to activate said data latch to capture data.

30. The method of claim 29 further comprising receiving said pointer strobe at a write state machine, said write state machine to sequentially activate and deactivate select signals in response to transitions on said pointer strobe.

31. The method of claim 30 further comprising receiving said timing strobe at latch enable logic, said latch enable logic to provide a latch pulse to selected data latch based on a logical combination of said select signals and said timing strobe.

32. The method of claim 31 wherein said pointer strobe and said timing strobe are dissimilar versions of said strobe signal.

33. The method of claim 32 wherein said pointer strobe and said timing strobe have dissimilar signal timing.

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# United States Patent [19]

Agoston

[11] Patent Number: 4,678,345

[45] Date of Patent: Jul. 7, 1987

## [54] EQUIVALENT TIME PSEUDORANDOM SAMPLING SYSTEM

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[21] Appl. No.: 858,424

[22] Filed: May 1, 1986

[51] Int. Cl.<sup>4</sup> ..... G04F 8/00; G03K 21/32[52] U.S. Cl. .... 368/119; 368/120;  
377/20; 324/77 R[58] Field of Search ..... 368/113, 118-120;  
324/77 R, 77 A, 77 C; 307/516; 364/484, 487;  
377/19, 20

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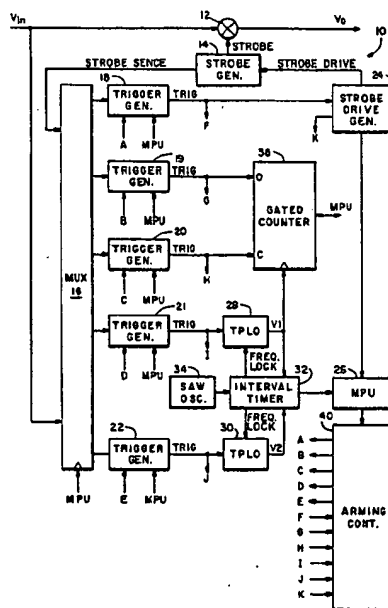
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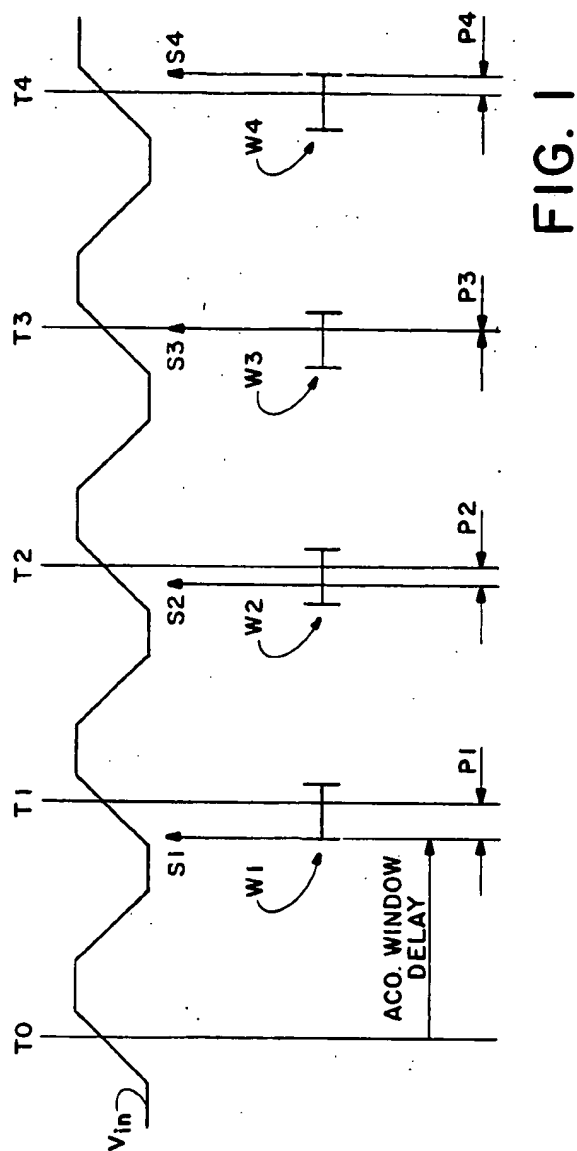
Primary Examiner—Vit W. Miska  
 Attorney, Agent, or Firm—John Smith-Hill; George T. Noe

## [57] ABSTRACT

An equivalent time pseudorandom sampling system samples a repetitive waveform within each of several narrow acquisition windows bounding repetitive sections of the waveform in order to obtain equivalent time sample data characterizing the shape of the waveform included within the acquisition windows. The period between successive triggering events is measured and sampling is delayed following an initiating triggering event by delay time adjusted according to the measured period so as to maximize the probability that sampling will occur within an acquisition window. The time difference between samples and subsequent triggering event is measured with high accuracy and resolution utilizing a time interval measurement system based on a dual vernier interpolation.

13 Claims, 6 Drawing Figures





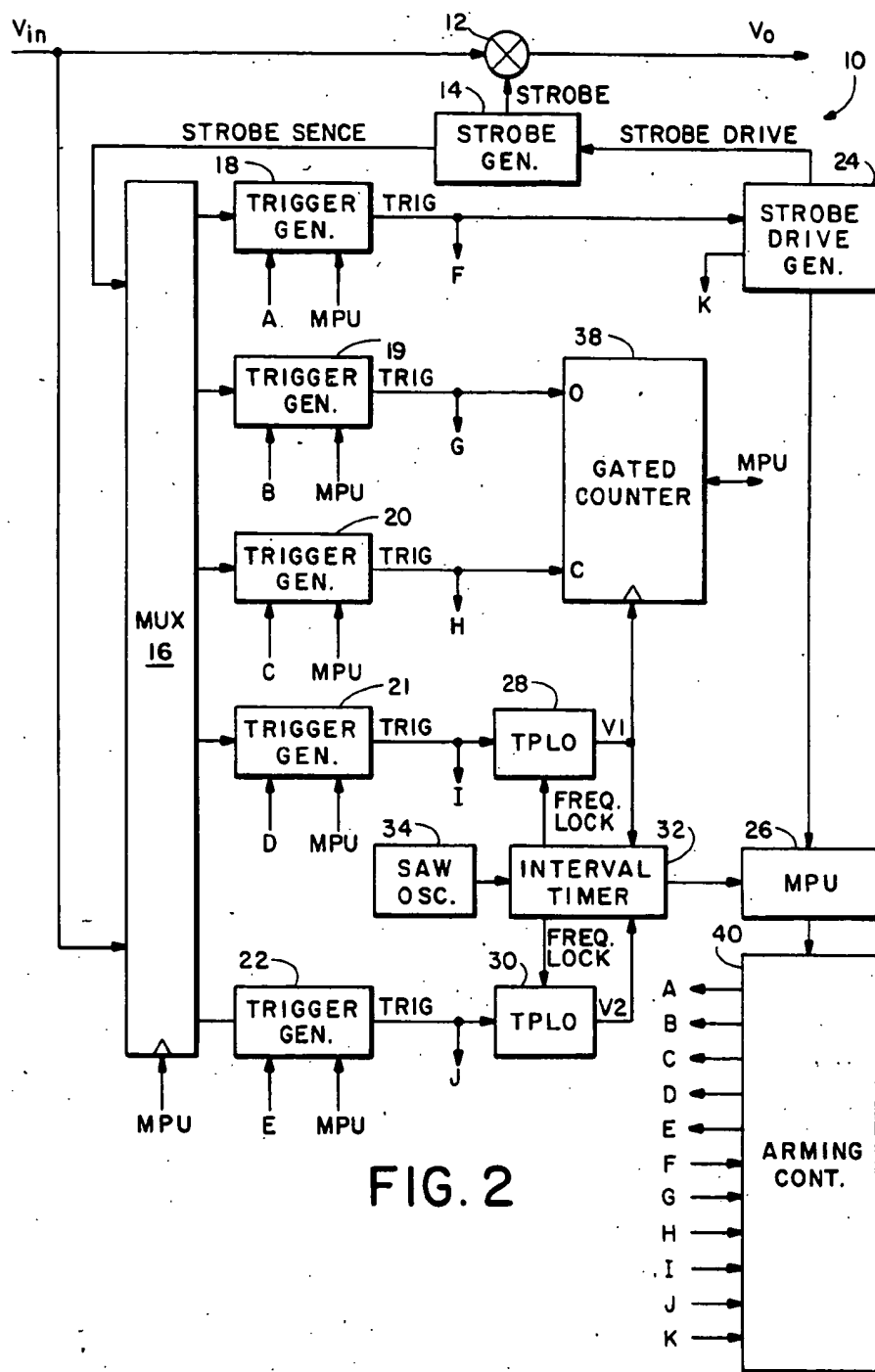
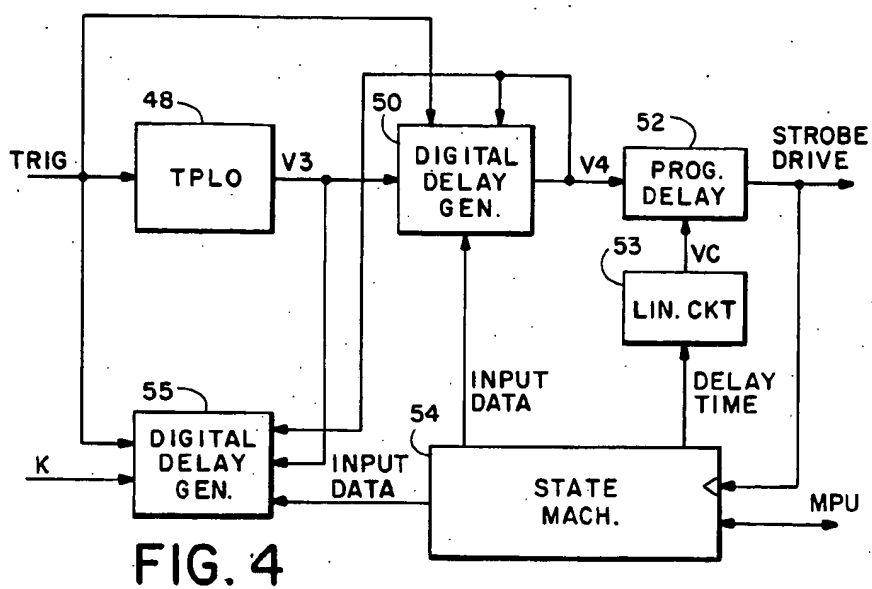
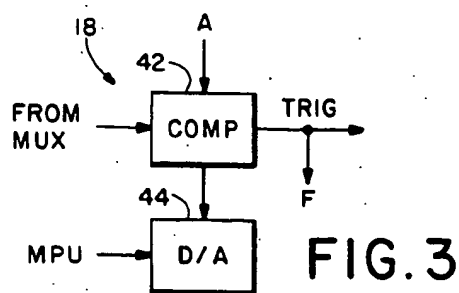


FIG. 2



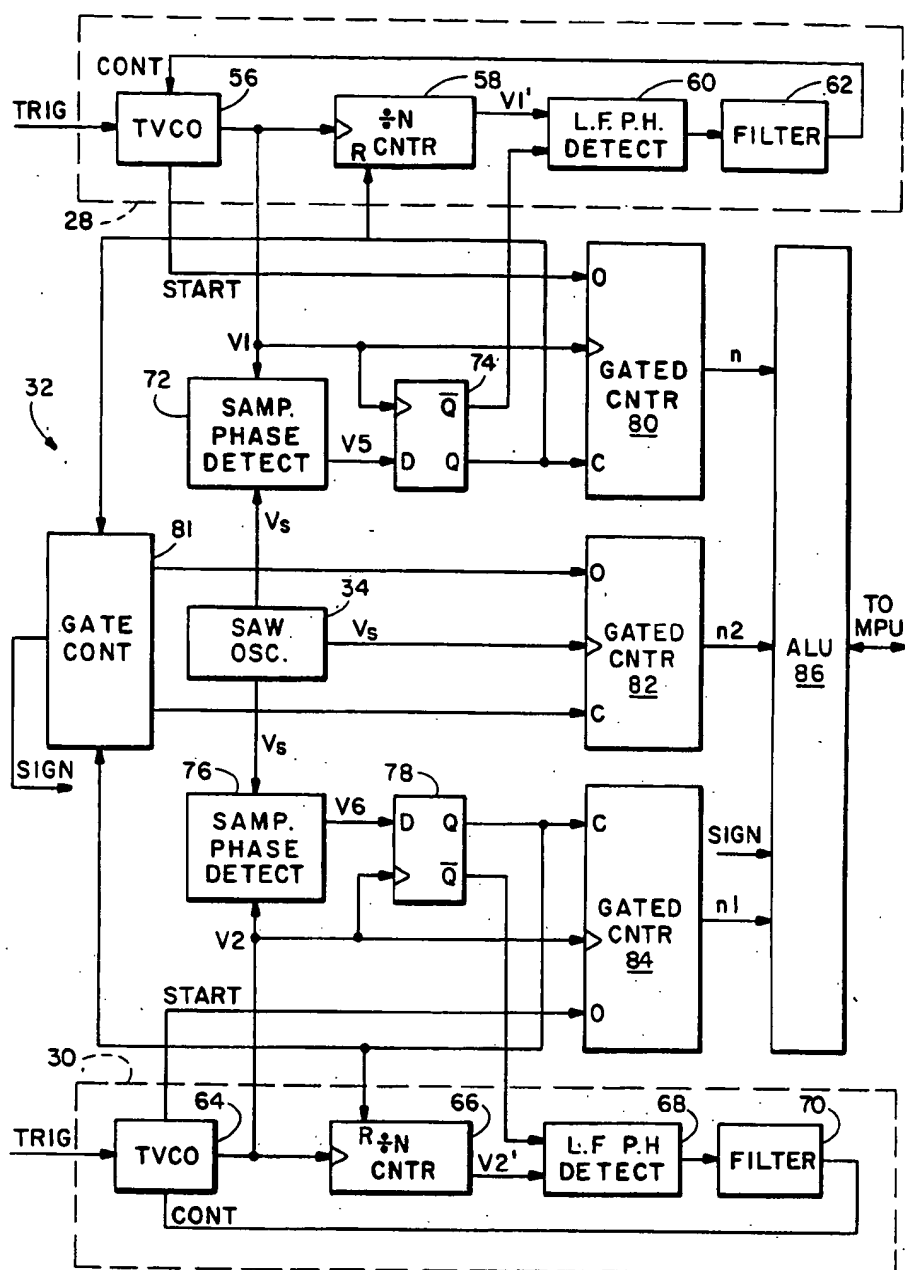


FIG. 5



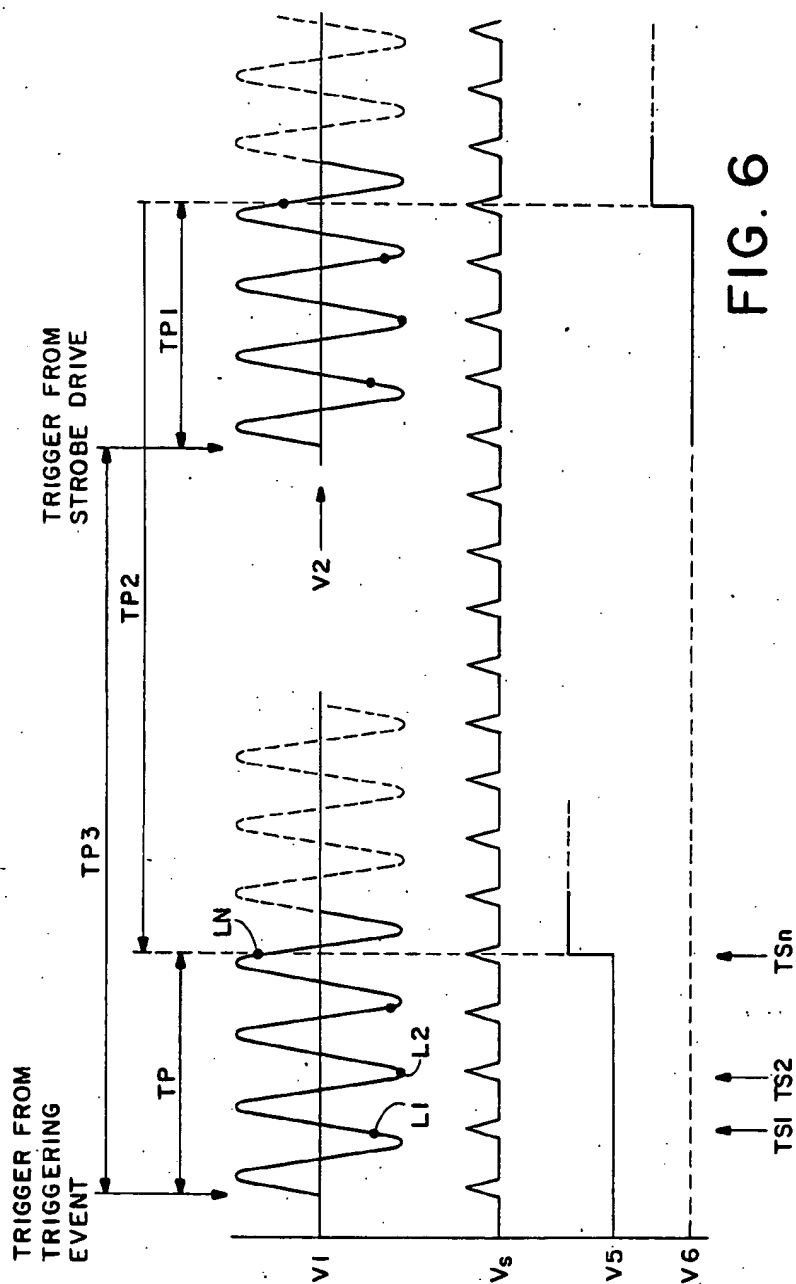


FIG. 6

## EQUIVALENT TIME PSEUDORANDOM SAMPLING SYSTEM

### BACKGROUND OF THE INVENTION

The present invention relates in general to waveform sampling systems and more particularly to a pseudorandom sampling system wherein a repetitive waveform is sampled at a predetermined time following a triggering event in a waveform and wherein the time interval between the sample and a subsequent triggering event is accurately measured.

A typical waveform sampling system repetitively strobes a sampling gate to sample a waveform at several points and the analog samples obtained are converted into digital data and stored in memory. In order to accurately characterize the shape of a sampled waveform, sample data should convey not only the magnitude of each waveform sample but the relative timing of each sample with respect to a triggering event (such as a zero crossing) in the waveform. Sequential and random sampling systems each provide timing information in a different way. Sequential sampling systems typically sample the waveform at predetermined regular time intervals following a triggering event in the waveform being sampled. The sampled waveform magnitude data is stored in memory in the order that it is acquired and since the sample timing is regular and predetermined, the position of the sample data in the memory is indicative of relative timing. In random sampling systems, sampling strobe signals are not synchronized to triggering events in the waveform and therefore the timing of each sampling strobe is "random" with respect to triggering events and not predetermined. Thus in random sampling systems it is necessary to measure the time interval between each sample and a triggering event in the waveform in order to determine the relative timing of each sample. The measured timing data is stored in memory along with the sampled waveform magnitude data.

Sampling systems are also characterized as to whether they perform real time or equivalent time sampling. In real time sampling systems a single section of a waveform is sampled and the resolution of the sampling, i.e., the maximum time between samples, depends entirely on the sampling frequency. Real time sampling is most suitable for non-repetitive or relatively low frequency periodic waveforms.

The equivalent time sampling method is used to obtain data characterizing a repeating section of a relatively high frequency, repetitive waveform. In equivalent time sampling, the waveform is sampled one or more times during each of several successive "acquisition windows", each acquisition window comprising a time period bounding a different repetition of the particular section of the waveform to be sampled. In sequential equivalent time sampling systems, a repetitive triggering event in the waveform occurring at some known time with respect to each acquisition window initiates sampling during each acquisition window. The initiation of sampling is delayed by differing predetermined times after each triggering event so that sampling occurs at different relative times within each acquisition window. The sample data is then ordered according to the relative sampling time within an acquisition window rather than according to the actual order in which the sample data was acquired. In random equivalent time sampling systems, sampling times and triggering events

are not synchronized but the time interval between samples within each acquisition window and a triggering event associated with the window is measured.

The resolution of sequential sampling systems depends on the resolution in control over sample timing delay while the resolution of random sampling systems depends on the resolution in measurement of the time differences between sampling strobes and triggering events. In sequential equivalent time sampling the timing of each sample is predetermined and there is essentially a one hundred percent probability that each sample will be taken within an acquisition window. However in random equivalent time sampling systems, the timing of each sample is not predetermined and many samples may be taken outside the intended acquisition window and must be discarded. The controllability of sample timing within an acquisition window afforded by sequential sampling permits samples to be taken at evenly spaced relative times within the acquisition windows such that a minimum number of samples are required to obtain a given resolution while in random sampling systems samples are not necessarily evenly spaced and more samples must be taken in order to achieve the same degree of resolution. Therefore when the sampling frequency for random and sequential equivalent time sampling is comparable, the random sampling method requires more time to achieve a desired degree of sampling resolution than sequential sampling.

Due to practical limitations of sequential sampling strobe drive circuitry, a triggering event must precede an acquisition window by a certain amount of time. If the triggering event is in the acquisition window, samples cannot be taken before the triggering event and therefore the entire window cannot be sampled. A triggering event occurring during one acquisition window may be utilized to trigger sampling for a subsequent acquisition window. However in such systems waveform "jitter" reduces sampling accuracy. Not all repetitive waveforms are periodic since the time between repetitive waveform sections in "jittery" waveforms may vary and the sample timing within an acquisition window may vary from expectations if the triggering event occurs outside the acquisition window. Consequently, in many equivalent time sequential sampling systems the sampled waveform is delayed following trigger pickoff, before being applied to the sampling gate, so that a triggering event within an acquisition window may be utilized to trigger sampling over the full range of the sample of the acquisition window. However, delay circuits may distort some waveforms to an intolerable degree and must be periodically measured to ensure that the delay time is accurately known.

What is needed is a method and apparatus for sampling a waveform with high resolution and high speed which is not subject to error due to waveform jitter and which does not require the delay of the waveform being sampled.

### SUMMARY OF THE INVENTION

In accordance with one aspect of the invention an equivalent time pseudorandom sampling system samples a repetitive waveform within each of several narrow acquisition windows positioned at similar times with respect to similar triggering events along the waveform in order to obtain equivalent time sample data characterizing the shape of a waveform section

included within each acquisition window. The period between successive triggering events is measured and sampling is delayed following an initiating triggering event by a delay time which is adjusted according to the measured period between triggering events so as to maximize the probability that sampling will occur within an acquisition window. The time difference between each sample and a triggering event within or near the acquisition window bounding the sample is then measured in order to accurately determine the timing of the sample with respect to the triggering event. The equivalent time pseudorandom sampling system of the present invention improves the data acquisition speed over prior art equivalent time random sampling systems by maximizing the number of samples taken within an acquisition window. The effect of waveform jitter is reduced by accurately measuring sample timing with respect to triggering events and there is no need to delay the waveform between trigger pickoff and sampling.

In accordance with another aspect of the invention, the relative timing within an acquisition window of each successive sample is delayed by regularly increasing time intervals so that samples are taken at substantially evenly spaced relative times within the acquisition windows, thereby minimizing the number of samples required to achieve a given sampling resolution.

In accordance with another aspect of the invention, the time intervals between waveform samples and triggering events are measured with high accuracy utilizing a novel time interval measurement system based on dual vernier interpolation. The strobe and triggering events each trigger the periodic output signal of a separate triggerable oscillator, each operating at a frequency differing slightly from the frequency of a surface acoustic wave (SAW) generator which periodically produces a reference signal. The triggering of one triggerable oscillator starts a count of the SAW generator output signals while the triggering of the other triggerable oscillator stops the count. The completed count is thus a gross measurement of the time interval between the strobe and the trigger. The phase differences between the first SAW strobe signal counted and the triggering of the first oscillator and between the last SAW strobe signal counted and the triggering of the second oscillator are also measured and used to finely adjust the measured time interval between the triggering events and strobe signals.

It is accordingly an object of the invention to provide an new and improved pseudorandom equivalent time waveform sampling system capable of sampling high speed repetitive waveforms with high accuracy, high resolution and high speed.

The subject matter of the present invention is particularly pointed out and distinctly claimed in the concluding portion of this specification. However, both the organization and method of operation, together with further advantages and objects thereof, may best be understood by reference to the following description taken in connection with accompanying drawings, wherein like reference characters refer to like elements.

### DRAWINGS

FIG. 1 shows a timing diagram depicting the operation of the equivalent time pseudorandom time sampling system according to the present invention;

FIG. 2 is a block diagram of the equivalent time pseudorandom time sampling system according to the present invention;

FIG. 3 is a block diagram of a typical trigger generator of the sampling system of FIG. 2;

FIG. 4 is a block diagram of the strobe drive generator circuit of FIG. 2;

FIG. 5 is a block diagram showing the phase locked oscillators and the interval timer of FIG. 2 in more detail; and

FIG. 6 shows a timing diagram of the operation of the phase detectors of FIG. 5.

### DETAILED DESCRIPTION

FIG. 1 shows a timing diagram illustrating equivalent time pseudorandom sampling according to the present invention. A repetitive input waveform  $V_{in}$  is sampled during each of four successive acquisition windows (W1-W4), each coinciding with a separate instance of a repetitive section of the input waveform. Each of four waveform samples is initiated by one of a sequence of four sampling strobes (S1-S4). In the example of FIG. 1, strobe S1 occurs at the beginning of acquisition window W1, strobe S2 occurs after the beginning of acquisition window W2 (about one-third of the time through the window), strobe S3 occurs within window W3 (about two-thirds of the time through the window), and strobe S4 occurs at the end of acquisition window W4. If each waveform sample is converted into a representative digital quantity and stored in memory, the stored data can be utilized to recreate the approximate shape of the waveform section within the acquisition windows, provided that the relative timing of each sample within an acquisition window is known. Accordingly the times (P1-P4) between each strobe signal S1-S4 and a corresponding triggering event T1-T4 (such as a zero crossing in the input waveform) occurring within or near the same acquisition window as the corresponding strobe signal is measured. This measured time interval may also be stored in memory along with the waveform magnitude data, and when the magnitude and timing data are displayed as dots on a screen with each dot having a vertical elevation proportional to the corresponding sample magnitude data and a horizontal position proportional to the measured timing data, the result approximates the shape of the waveform during the acquisition window.

The strobe signals are initiated in delayed response to a triggering event. For instance, strobe signal S1 is initiated in response to a triggering event T0 occurring in the input waveform  $V_{in}$  during a cycle of the waveform preceding acquisition window W1. Similarly, strobe signal S2 is generated in delayed response to triggering event T1, strobe S3 is generated in response to triggering event T2 and strobe S4 is generated in response to triggering event T3. According to the present invention, the delay between a triggering event and the strobe that it initiates is adjusted so that the strobe is most likely to occur within the corresponding sampling window and so that the position of each successive strobe is progressively delayed by a regular amount of time with respect to the triggering event. In order to determine the acquisition window delay time, i.e., the time between a triggering event and the next section of the waveform to be sampled, the period between triggering events (not shown) occurring before triggering event T0 is measured and used as a predictor of when triggering events T1-T4 will occur with respect to

triggering event T0. The delay times between triggering events T0-T3 and strobe signals S1-S4, respectively, are then adjusted so that strobe signals S1-S4 are generated at predetermined, regularly incremented times with respect to the predicted timing of corresponding triggering events T1-T4. Although for simplicity the example of FIG. 1 shows only four strobes, many more samples may be taken, the relative sampling times of successive samples being progressively increased by smaller amounts to provide higher sampling resolution.

The use of the premeasured time interval between prior triggering events as a predictor of the time interval between subsequent triggering events enables strobe signal timing to be controlled so as to maximize the probability that each strobe signal will be generated within an acquisition window, even when the acquisition window is relatively narrow. By subsequently measuring the actual time interval between each strobe signal and a triggering event within or near the acquisition window to determine the actual timing of each strobe, the effect of input waveform jitter on sampling accuracy is minimized.

Referring to FIG. 2, depicting in block diagram form the equivalent time pseudorandom sampling system 10 according to the present invention, sampling system 10 includes a sampling gate 12 for sampling the input waveform Vin on each occurrence of a strobe signal in order to produce an output voltage sample Vo. The strobe signal is generated by a strobe generator 14 in response to an input strobe drive signal. At the same time, strobe generator 14 also generates a strobe sense signal which is applied as an input to a multiplexer 16. The Vin signal is also provided to another input of multiplexer 16. Multiplexer 16 has five outputs, each connected to a separate trigger generator 18-22, and the multiplexer is adapted to selectively connect any one of its inputs to any one or more of the trigger generators.

The triggering event recognized by trigger generators 18-22 is the crossing of a predetermined level by an input waveform, the level being determined by data supplied by microprocessor 26. When generator 18 produces an output trigger signal in response to a triggering event in an input signal from multiplexer 16, its output trigger signal is transmitted to a strobe drive generator 24. After a predetermined delay time following the trigger signal produced by trigger generator 18, strobe drive generator 24 produces the strobe drive signal which initiates operation of the strobe generator 14.

When trigger generator 21 produces an output trigger signal in response to a predetermined triggering event in its input signal, this trigger signal triggers a triggered phase-locked oscillator (TPLO) 28. On receipt of the trigger signal from trigger generator 21, TPLO 28 stops and restarts its periodic output signal V1 such that the V1 signal is synchronized to the trigger signal. The trigger signal output of trigger generator 22 is applied as a triggering input to another TPLO 30 which also stops and restarts its periodic output signal V2 in response to the triggering input. The V1 output signal of TPLO 28 and the V2 output signal of TPLO 30 are applied as inputs to an interval timer circuit 32 adapted to measure the time interval between the restarting of the V1 and V2 signals and to provide data indicating the measured time intervals to a microprocessor (MPU) 26. A surface acoustic wave (SAW) oscillator 34 provides a reference signal which interval timer

circuit 32 utilizes when determining the time interval between the triggering of TPLO 28 and TPLO 30. The interval timer circuit also provides signals which frequency lock the V1 and V2 signals to predetermined frequencies using the SAW oscillator 34 frequency as a reference.

The trigger signal outputs of trigger generators 19 and 20 are connected to gate open (O) and gate close (C) inputs of a gated counter 38. Counter 38 counts the cycles of the output signal V1 from TPLO 28 which occur after the trigger signal produced by trigger generator 19 and before the trigger signal produced by trigger generator 20. The count data is then provided to microprocessor 26.

Each trigger generator 18-22 is armed by a signal from an arming controller 40, suitably comprising a state machine programmed by data from microprocessor 26, and each trigger generator 18-22 transmits an indicating signal to arming controller 40 whenever it detects a triggering event.

In order to measure the period between successive triggering events in the Vin waveform, microprocessor 26 switches multiplexer 16 so that it supplies the Vin waveform as input to both trigger generators 19 and 20 and programs arming controller 40 to alternately arm trigger generators 19 and 20. After trigger generator 19 detects a triggering event in the Vin waveform, it generates its trigger signal output to start the count of cycles of the V1 output signal of TPLO 28 by period counter 38. Trigger generator 19 also transmits a signal to the arming controller 40 indicating that the triggering event has been recognized. In response to the indicating signal, the arming controller 40 immediately disarms trigger generator 19 and arms trigger generator 20 so that trigger generator 20 generates its output trigger signal on detection of the next triggering event in the Vin waveform in order to stop the count of period counter 38. When the trigger generator 20 transmits its indicating signal back to the arming controller 40, the arming controller sends a signal to the microprocessor telling it that it may read and reset the count in period counter 38. The period between the successive triggering events can be determined by dividing the count by the frequency of the V1 signal output of TPLO 28.

The microprocessor 26 then utilizes the measured period data when setting the delays between the trigger output of trigger generator 18 and the strobe drive signal produced by strobe drive generator 24 so as to properly time the strobe signals applied to the sampling gate 12. The microprocessor also supplies count limit data to each trigger generator 18-20 which tells the trigger generator to initiate a trigger signal only after a predetermined number of trigger signals have been generated. Thus, for instance, if trigger generator 20 is told to initiate a trigger only after detecting 10 trigger signals, the resulting count produced by counter 38 can be used to determine an average period between triggering events. The use of an averaging measurement is preferable when the input waveform is subject to random jitter.

Prior to an equivalent time pseudorandom sampling operation, microprocessor 26 sets trigger generator 21 to detect a predetermined triggering event in the Vin waveform and sets trigger generator 22 to detect the occurrence of the strobe sense signal produced by strobe generator 14 so that interval timer 32 measures the time intervals between triggering events and strobe sense signals. Referring to both FIGS. 1 and 2, the

initial triggering event T0 causes trigger generator 18 to transmit its output trigger signal to strobe drive generator 24 which produces a strobe drive signal at a predetermined delay time following the trigger signal, the delay time being predetermined by data previously supplied to the strobe drive generator 24 by the microprocessor 26. The strobe drive signal causes the strobe generator 14 to generate strobe signal S1 along with a strobe sense signal. The strobe sense signal is transmitted through multiplexer 16 to the trigger generator 22 which causes trigger generator 22 to trigger (stop and restart) the output of TPLO 30. When the output signal V2 of TPLO 30 is triggered, interval timer 32 begins an interval measurement. On detection of triggering event T1, trigger generator 21 produces its output trigger signal which triggers the V1 output signal of TPLO 28 thereby marking the end of the interval measured by interval timer 32. Thus the interval timer 32 measures the time interval P1 of FIG. 1 between the strobe signal S1 and the triggering event T1.

The triggering event T1 also causes trigger generator 18 to produce another trigger signal provided to strobe drive generator 24 causing strobe drive generator 24 to produce a second strobe drive signal in order to initiate strobe signal S2. The timing between triggering event T1 and strobe signal S2 is also determined by data previously provided to the strobe drive generator 24 by the microprocessor 26. When strobe generator 14 produces strobe signal S2 it produces a second strobe sense signal which is transmitted through multiplexer 16 to trigger generator 22 thereby causing trigger generator 22 to initiate a second triggering signal, retriggering the TPLO 30, and starting another time interval measurement. When trigger generator 21 detects triggering event T2, it retriggers TPLO 28 to mark the end of the interval measured by interval timer 32. Thus the output of interval timer 32 now represents the period P2 between the strobe signal S2 and the triggering event T2. The process continues such that the interval timer 32 successively measures the period P3 between the strobe signal S3 and event T3 and the period P4 between the event T4 and the strobe signal S4. The interval timer 32 is adapted to measure the interval between the initiation of V1 and V2 regardless of which signal is initiated first. Therefore in the case of period P4 between the triggering event T4 and the strobe signal S4, the triggering of TPLO 28 initiates interval measurement while the triggering of TPLO 30 in response to the strobe sense signal terminates the interval measurement.

Referring to FIG. 3, depicting in more detailed block diagram form trigger generator 18 of FIG. 2, the trigger generator includes a comparator 42 for producing an output pulse the first time the magnitude of the output signal from the multiplexer 16 of FIG. 2 rises above an output signal of a digital-to-analog converter 44 following receipt of an arming signal A from the arming controller 40 of FIG. 2. The magnitude of the output signal of converter 44 is determined by data from the microprocessor 26 of FIG. 2. The trigger signal output of comparator 42 is applied as an input F to the arming controller 40 of FIG. 2. Trigger generators 19-22 are similar to trigger generator 18 of FIG. 3.

A strobe drive circuit suitable for use as strobe drive generator 24 of FIG. 2 is described in detail in co-pending U.S. patent application Ser. No. 06/858,490 filed Apr. 30, 1986. Referring to FIG. 4, depicting in more detailed block diagram form the strobe drive generator 24 of FIG. 2, strobe drive generator 24 includes a trig-

gered phase-locked oscillator (TPLO) 48 which stops and restarts a periodic output signal V3 when triggered by a trigger signal produced by trigger generator 18 of FIG. 2. The trigger signal is also applied to an enable input of a low jitter digital delay generator 50 similar to a delay generator described in copending U.S. patent application Ser. No. 06/845,282 filed Mar. 28, 1986. The V3 output signal of TPLO 48 is applied to a count input of delay circuit 50 and when the trigger signal is asserted, the delay circuit begins decrementing a pre-stored number, the number being decremented by one on each cycle of the V3 signal. When the stored number reaches zero, the delay circuit 50 outputs a pulse V4 to a programmable delay circuit 52. Delay circuit 52 delays the V4 pulse by a delay time determined by an applied control voltage Vc in order to produce the strobe drive output signal of the strobe drive generator 24. The V4 pulse is also fed back to a data load input of delay generator 50 which causes delay generator 50 to stop counting and to load a new number for starting a new count down when enabled by the next occurrence of a trigger signal.

The input data for the delay generator 50 and the predetermined delay time of programmable delay circuit 52 are controlled by data from the state machine 54 which is clocked by the strobe drive signal. The delay time data output of state machine 54 is converted to the control voltage Vc by a linearizing circuit 53 adapted to linearize changes in time delay of delay circuit 52 with respect to changes in delay time data provided by state machine 54. A circuit suitable for use as programmable delay circuit 52 is described in co-pending patent application Ser. No. 06/846,320 filed Mar. 31, 1986 and a circuit suitable for use as linearizing circuit 53 is described in co-pending patent application Ser. No. 06/846,319 filed Mar. 31, 1986.

The input data applied to delay generator 50 grossly adjusts strobe delay while the delay time data transmitted to linearizing circuit 53 finely adjusts the strobe delay. Prior to a sampling operation, but after determining the nominal period between successive triggering events, microprocessor 26 of FIG. 2 programs state machine 54 to properly adjust the delays between successive trigger signals and the output strobe drive signal. In the example illustrated in FIG. 1, state machine 54 is programmed to step through four separate states, one for each strobe signal. While in a first state, state machine 54 generates delay control data sufficient to provide the appropriate delay between triggering event T0 in the input waveform Vin and the strobe signal S1. When the strobe drive signal initiating strobe signal S1 is generated by the programmable delay circuit 52, the strobe drive signal switches the state machine 54 to a second state in which the data output of the state machine increases the delay between the trigger and strobe drive signal to the interval required between triggering event T1 and strobe signal S2 as shown in FIG. 1. When the strobe drive signal initiating strobe signal S2 is produced, state machine 54 switches to a third state wherein the delay is increased once again to the time interval required between triggering event T3 and strobe signal S4 of FIG. 1. When the last strobe drive signal is generated, state machine 54 transmits a signal back to microprocessor 26 indicating the end of a sampling cycle.

The periodic output signal V3 of the TPLO 48 is also applied to the count input of another digital delay generator 55, similar to delay generator 50. The trigger

signal and the V4 signal are also applied to the count enable and data load control inputs of delay generator 55 and the state machine 54 also supplies input data to delay generator 55. When a V4 pulse is generated, delay generator 55 stores input data from state machine 54 and, when subsequently enabled by the trigger signal, begins decrementing the stored input data by one on each cycle of the V3 signal. When the stored input data is decremented to zero, delay generator transmits an indicating signal K to the arming controller 40 of FIG. 2. The arming controller then transmits an arming signal A to the trigger generator 18 of FIG. 2, which permits the trigger generator to produce another trigger signal on occurrence of the next triggering event. The input data provided to delay generator 55 is adjusted to prevent trigger generator 18 from retriggering the TPLO 48 until a strobe drive signal has been generated in response to the last trigger signal. This feature is necessary when a very high frequency waveform is being sampled and not every triggering event is to initiate a sampling strobe.

Referring to FIG. 5 depicting in more detailed block diagram form the triggered phase-locked oscillators 28 and 30 and the interval timer circuit 32 of FIG. 2, TPLO 28 includes a triggered, voltage-controlled oscillator (TVCO) 56, a divide-by-N counter 58, low frequency phase detector 60, and a filter circuit 62. The trigger signal from the trigger generator 21 of FIG. 2 triggers TVCO 56 which stops and restarts the V1 output signal of the TPLO 28 so as to synchronize the V1 signal to the trigger signal. The V1 output signal clocks the divide-by-N counter 58 which produces an output signal V1' lower in frequency than V1 by a factor of N. The V1' signal is applied to the reference input of the low frequency phase detector 60 which produces an output signal equal to the difference in magnitude between the V1' signal and the frequency locking signal produced by the interval timer circuit 32. The output signal of the low frequency phase detector 60 is integrated by filter 62 and then applied to TVCO 56 as its frequency controlling voltage.

The V1 signal output of TVCO 56 and the output signal of SAW oscillator are applied as inputs to a sampling phase detection circuit 72. A circuit suitable for use as phase detector circuit 72 is described in detail in co-pending U.S. patent application Ser. No. 06/858,428 filed May 1, 1986 and a circuit suitable for use as saw oscillator 34 is described in detail in co-pending U.S. patent application Ser. No. 06/858,485 filed Apr. 30, 1986. Phase detection circuit 72 samples the V1 input waveform on each occurrence of a strobe output signal produced by the SAW oscillator 34 and produces an output signal V5 whenever the sampled V1 signal falls below zero potential. The output signal V5 is applied to a D input of a flip-flop 74 clocked by the V1 output signal of TVCO 56. The inverted Q output of flip-flop 74 provides the frequency-locking signal applied to a non-inverting input of phase detector 60 while the Q output of the flip-flop resets the divide-by-N counter 58.

The TVCO 56 operates continuously, the stopping and restarting of TVCO 56 by the trigger signal from trigger generator 18 of FIG. 2 being substantially instantaneous. In the preferred embodiment of the invention, the SAW oscillator 34 operates at a frequency of 315.457 megahertz and the count limit N of counter 58 is 4096. In this arrangement the frequency difference between the output Vs of the SAW oscillator 34 and the output V1 of TVCO 56 must be such that the output

signal V5 of phase detector 72 oscillates at the same frequency as the output V1' of divide-by-N counter 58. This occurs when the output signal of TVCO 56 is  $(N+1)/N$  times the frequency of the SAW oscillator output signal, i.e., when V1 is 315.380 megahertz.

Referring to FIG. 6, showing a timing diagram of the operation of phase detector 72, the phase detector is adapted to sample the V1 input waveform on each occurrence of strobe signal Vs output of SAW oscillator 34. Since the strobe signal Vs is of a slightly higher frequency than the oscillator output signal V1, the phase detector 72 samples the oscillator output signal at a progressively earlier point on each cycle of the output signal V1. In the example of FIG. 6 the first strobe signal Vs occurring after TVCO 56 of FIG. 3 receives a trigger signal causes the phase detector 72 to sample the TVCO output signal at time TS1 and the next strobe signal causes the phase detector 72 to sample the V1 signal at time TS2. The magnitude of the sample at time TS2 is higher than the sample at time TS1. With each successive strobe signal Vs, the sampled magnitude changes until time TSn when the sampled magnitude of the V1 signal rises above zero. At this point phase detector 72 transmits the V5 pulse to flip-flop 74 of FIG. 5. The number of cycles n of V1 occurring after the trigger signal but before phase detector 72 produces the V5 output signal are counted and the time difference TP between the trigger signal and the point of phase coincidence between the zero crossing of the V1 signal and the Vs signal at time Tn is computed by multiplying n by the step size of the relative phase shift between Vs and V1 after each cycle of V1. In the preferred embodiment of the invention, with Vs at a frequency of 315.457 megahertz and with V1 at a frequency of 315.380 megahertz, the step size and therefore the resolution of the measurement is 0.774 picoseconds. Thus, for example, if n is 100, TP is about 77.4 picoseconds. In FIG. 6 the difference in frequency between the Vs and V1 signals has been exaggerated for illustrative purposes so that the step size is large enough to illustrate the stepping of the sample timing relative to the phase of V1.

Referring again to FIG. 5, TPLO 30 is similar to TPLO 28 and includes a triggered voltage controlled oscillator 64 driving a divide-by-N counter 68, triggered low frequency phase detector 68, and a filter 70, the output of filter 70 being fed back to the frequency control input of TVCO 64. The output of TVCO 64 comprises the V2 signal output of the TPLO 30 which is applied to another sampling phase detector 76, similar to phase detector 72. The output of phase detector 76 is applied to a D input of another flip-flop 78, the inverted Q output of flip-flop 78 being connected as the frequency locking signal to the low frequency phase detector 68. The divide-by-N counter 66 is also set with a count limit of N equal to 4096 and the output strobe signal Vs of SAW oscillator 34 is applied as the strobe signal to phase detector 76. In this arrangement the output signal V2 of TVCO 64 is also maintained at 315.380 megahertz.

The interval timer 32 also includes a set of three gated counters 80, 82 and 84, each having a gate-open control input (O), a gate-close control input (C), and a clock input. Each gated counter counts the number of cycles applied to its clock input following a pulse applied to the gate-open input, the count being terminated by a pulse applied to the gate-close input. The output Vs of SAW oscillator 34 is applied to the clock input of gated counter 82, the output V1 of TVCO 56 is applied to the

clock input of gated counter 80 and the output V2 of TVCO 64 is applied to the clock input of gated counter 84. The Q output of flip-flop 74 drives the gate-close terminal of gated counter 80 and the Q output of flip-flop 78 drives the gate-close terminal of gated counter 84. TVCO 56 generates a start signal pulse whenever the trigger generator 18 of FIG. 2 retriggers the output signal V1 of TVCO 56 and the start signal is applied to the gate-open input of counter 80. A similar start signal generated by TVCO 64 is also applied to the gate-open input of counter 84. The Q outputs of flip-flops 74 and 78 are connected to inputs of a gate control circuit 81. Gate control circuit 81 has three outputs, one driving the gate-open input of counter 82, another driving the gate-close input of counter 82 and a third (SIGN) indicating whether the Q output of flip-flop 74 sets before or after the Q output of flip-flop 78. The gate control circuit 81 is a state machine which asserts its gate-open output when the first of either of the Q outputs of flip-flop 74 or 78 is set and asserts its gate-close output when the second Q output sets.

Assuming by way of example that the time difference between a triggering event and a strobe signal is to be measured and that the triggering event appears before the strobe signal, the triggering event detected by trigger generator 21 of FIG. 2 causes the trigger generator 21 to transmit a trigger signal to TVCO 56 of TPLO 28 before the strobe sense signal produced by strobe generator 14 causes trigger generator 22 to transmit a trigger signal to TVCO 56 of the TPLO 30. When the TVCO 56 is triggered, it transmits its start signal to the gate-open terminal of gated counter 80. Gated counter 80 thereupon begins counting cycles of the V1 output signal of TVCO 56. When phase detector 72 detects a next zero crossing in the sampled value of V1, it sets flip-flop 74. The Q output of flip-flop 74 pulses the gate-close input of counter 80 to terminate the count. Thus the ending count n in gate counter 80 represents the time period TP of FIG. 6 between the trigger signal applied to TVCO 56 and the next coincidence between a zero crossing of V1 and a strobe signal Vs. When the gate control circuit 81 detects the Q output of flip-flop 74, it transmits a pulse to the gate-open terminal of counter 82 causing counter 82 to begin counting pulses of the Vs signal output of the SAW oscillator 34.

The trigger signal resulting from the strobe sense signal retriggers TVCO 64 and TVCO 64 generates a start signal pulse which gate opens counter 84 so that counter 84 begins counting pulses of the V2 signal. Phase detector 76 samples the V2 signal produced by TVCO 64 and when it detects a next zero crossing in the sampled value of V2, it sets flip-flop 78. The Q output of flip-flop 78 pulses the gate-close input of counter 84 to terminate its count. Thus the ending count n1 in gated counter 80 represents the time period TP1 of FIG. 6 between the trigger signal applied to TVCO 64 and the next coincidence between a zero crossing of V2 and a strobe signal Vs. When the gate control circuit 81 detects the Q output of flip-flop 78, it transmits a pulse to the gate-close terminal of counter 84 causing counter 84 to stop counting pulses of the Vs signal output of the SAW oscillator 34. The ending count n2 in counter 82 thus is indicative of the period TP2 between the V5 pulse and the V6 pulse. The time period TP3 between the triggering event and the strobe sense signal may be computed according to the following expression:

$$TP3 = Tsaw \{ (n2) + [(N+1)(n1 - n)/N] \} \quad (1)$$

where Tsaw is the period of the SAW oscillator 34 output signal Vs, N is the setting (4096) of the divide by N counters 58 and 66, n is the ending count in counter 80, n1 is the ending count in counter 84, and n2 is the ending count in counter 82.

When the strobe sense signal occurs before the triggering event, the period TP3 between the trigger signals generated in response to the strobe sense signal and the triggering event is determined by the expression:

$$TP3 = Tsaw \{ (n2) + [(N+1)(n1 - n)/N] \} \quad (2)$$

The count outputs n, n1 and n2 of gated counters 80, 84 and 82, along with the SIGN signal output of gate control circuit 81 are applied to an arithmetic logic unit (ALU) 86 which computes the above, depending on the state of the SIGN signal indicating whether the triggering event or the strobe drive signal occurred first. The ALU 86 then transmits the computed time to the microprocessor 26 of FIG. 2.

The interval timer 32 may also be utilized to measure jitter in the Vin signal with a high degree of accuracy. Referring to FIGS. 1 and 2, when a repetitive signal such as Vin is subject to jitter, the period between successive triggering events T0-T4 varies. To accurately measure the time period between successive triggering events the input signal Vin may be applied to both trigger generator 21 and trigger generator 22 of FIG. 2 and the trigger generators 21 and 22 may be successively armed by arming controller 40 so that trigger generator 21 generates a trigger signal on detection of a first triggering event in the input waveform Vin while trigger generator 22 generates a trigger signal on the second triggering event in the input waveform Vin. Thus interval timer 32 measures the time difference between the two triggering events with high accuracy. Signal jitter is determined by comparing measured time difference between successive pairs of triggering events.

Thus according to the foregoing description the equivalent time pseudorandom sampling system of the present invention samples a repetitive waveform within each of several acquisition windows bounding repetitive sections of the waveform. In order to obtain equivalent time sample data characterizing the shape of the waveform included within each acquisition window, the period between successive triggering events is measured and sampling is delayed following an initiating triggering event by delay times adjusted according to the measured periods so as to maximize the probability that sampling will occur within each acquisition window. The time intervals between samples and triggering events are measured with high accuracy utilizing the above-described dual vernier interpolation time interval measurement system.

While a preferred embodiment of the present invention has been shown and described, it will be apparent to those skilled in the art that many changes and modifications may be made without departing from the invention in its broader aspects. The appended claims are therefore intended to cover all such changes and modifications as fall within the true spirit and scope of the invention.

I claim:

1. A method for measuring a time interval between first and second events comprising the steps of:  
periodically generating a reference signal;

triggering first and second periodic signals on occurrence of said first and second events, respectively; sampling said first and second periodic signals on each occurrence of said reference signal and determining the magnitude of each signal sample; counting cycles of said first periodic signal occurring after triggering said first periodic signal and before the sampled magnitude of said first periodic signal crosses a predetermined level, thereby producing a first count; counting cycles of said second periodic signal occurring after triggering said second periodic signal and before the sampled magnitude of said second periodic signal crosses said predetermined level, thereby producing a second count; and counting occurrences of said reference signal generated between a first moment when said sampled magnitude of said first periodic signal crosses said predetermined level and a second moment when said sampled magnitude of said second periodic signal crosses said predetermined level, thereby producing a third count.

2. The method according to claim 1 wherein said first and second periodic signals are of frequencies which differ from the frequency of said reference signal.

3. The method according to claim 2 further comprising the step of computing said time interval according to said first, second and third counts.

4. A method for sampling a repetitive waveform, the method comprising the steps of:  
measuring a first time interval between first and second triggering events in said repetitive waveform; and  
generating in delayed response to a third triggering event in said repetitive waveform a strobe signal for initiating sampling of said repetitive waveform, the delay between said third triggering event and generation of said strobe signal being adjusted according to said measured time interval.

5. The method according to claim 4 wherein said delay is adjusted to equal the sum of said measured first time interval and a predetermined interval.

6. The method according to claim 4 wherein said delay is adjusted to equal the difference between said measured first time interval and a predetermined interval.

7. The method according to claim 4 further comprising the step of measuring a second time interval between said strobe signal and a fourth triggering event in said repetitive waveform.

8. The method according to claim 7 wherein the step of measuring said second time interval comprises the substeps of:  
periodically generating a reference signal;  
triggering a first periodic signal on occurrence of said strobe signal and triggering a second periodic signal on occurrence of said fourth triggering event;  
sampling said first and second periodic signals on each occurrence of said reference signal and determining the magnitude of each signal sample;  
counting cycles of said first periodic signal occurring after triggering said first periodic signal and before the sample magnitude of said first periodic signal crosses a predetermined level;  
counting cycles of said second periodic signal occurring after triggering said second periodic signal and before the sample magnitude of said second periodic signal crosses a predetermined level; and  
counting occurrences of said reference signal generated between a first moment when said sampled magnitude of said first periodic signal crosses said predetermined level and a second moment when

said sampled magnitude of said second periodic signal crosses said predetermined level.

9. An apparatus for measuring a time interval between first and second events comprising:  
a reference oscillator for periodically generating a reference signal;  
a first triggerable oscillator for generating a first periodic signal triggered by said first event;  
a second triggerable oscillator for generating a second periodic signal triggered by said second event;  
means for sampling said first and second periodic signals on each occurrence of said reference signal;  
means for counting cycles of said first periodic signal occurring before the sampled magnitude of said first periodic signal crosses a predetermined level;  
means for counting cycles of said second periodic signal occurring before the sampled magnitude of said second periodic signal crosses a predetermined level; and  
means for counting occurrences of said reference signal generated between a first moment when said sampled magnitude of said first periodic signal crosses said predetermined level and a second moment when said sampled magnitude of said second periodic signal crosses said predetermined level.

10. An apparatus for timing sampling of a repetitive waveform comprising:  
means for measuring a first time interval between first and second triggering events in said repetitive waveform; and  
means for generating in delayed response to a third triggering event in said repetitive waveform a strobe signal for initiating sampling of said repetitive waveform, the delay between said third triggering event and generation of said strobe signal being set according to said measured first time interval.

11. The apparatus according to claim 10 wherein said delay is set equal to said measured first time interval adjusted by a predetermined interval.

12. The apparatus according to claim 10 further comprising means for measuring a second time interval between said strobe signal and a fourth triggering event in said repetitive waveform.

13. The apparatus according to claim 12 wherein said means for measuring said second time interval comprises:  
means for periodically generating a reference signal;  
a first triggerable oscillator for generating a first periodic signal when triggered by said strobe signal;  
a second triggerable oscillator for generating a second periodic signal when triggered by said fourth triggering event;  
means for sampling said first and second periodic signals on each occurrence of said reference signal;  
means for counting cycles of said first periodic signal occurring after triggering of said first periodic signal and before the sampled magnitude of said first periodic signal crosses a predetermined level;  
means for counting cycles of said second periodic signal occurring after triggering of said second periodic signal and before the sampled magnitude of said second periodic signal crosses said predetermined level; and  
means for counting occurrences of said reference signal generated after a first moment when said sampled magnitude of said first periodic signal crosses said predetermined level and a second moment when said sampled magnitude of said second periodic signal crosses said predetermined level.

\* \* \* \* \*





US006640193B2

(12) **United States Patent**  
Kuyel

(10) Patent No.: **US 6,640,193 B2**  
(45) Date of Patent: **Oct. 28, 2003**

(54) **METHOD AND SYSTEM FOR MEASURING JITTER**

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(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 133 days.

(21) Appl. No.: **09/731,433**

(22) Filed: **Dec. 6, 2000**

(65) **Prior Publication Data**

US 2002/0103609 A1 Aug. 1, 2002

**Related U.S. Application Data**

(60) Provisional application No. 60/171,260, filed on Dec. 15, 1999.

(51) Int. Cl.<sup>7</sup> ..... **G06F 19/00**

(52) U.S. Cl. .... **702/69; 702/32; 702/57; 702/106; 714/751; 714/758; 375/226; 375/227; 370/516; 370/503; 340/310.03; 340/146.2; 324/613; 324/620**

(58) Field of Search ..... **702/32, 57, 69-71, 702/74, 81, 82, 84, 85, 106, 112, 124-126, 189, 190; 324/600, 613-626, 76.19, 76.24, 76.38; 370/516, 503, 506, FOR 177, FOR 185; 375/226, 224, 227, 228; 714/751, 748, 746, 752, 758-762, 764, 765**

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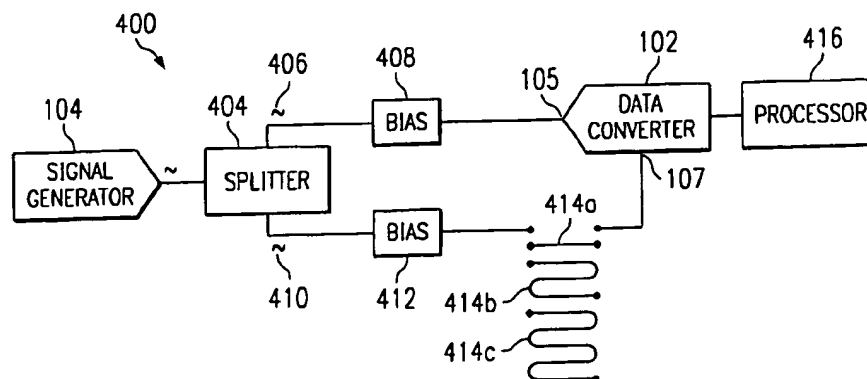
*Assistant Examiner*—Elias Desta

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(57) **ABSTRACT**

According to one embodiment of the present invention, a system (100) for measuring overall jitter is disclosed that includes a data converter (102) that measures a signal to generate a first measurement set (212) and a second measurement set (214), which are used to compute overall jitter. According to one embodiment of the present invention, a method for measuring overall jitter is disclosed. The data converter (102) generates the first measurement set (212) and the second measurement set (214) by measuring the signal. The overall jitter is computed using the measurement sets (212 and 214). According to one embodiment of the present invention, a system (400) for measuring internal jitter is disclosed that includes a splitter (404) that splits a signal into an input signal (406) and a clock signal (410). The data converter (102) measures the input signal (406) to generate a first data set and a second data set, which are used to compute the internal jitter of the data converter (102). According to one embodiment of the present invention, a method for measuring internal jitter is disclosed. A signal is split into an input signal (406) and a clock signal (410). The data converter (102) measures the input signal to generate the first data set (508) and the second data set (512). The internal jitter is computed using the first data set (508) and the second data set (512). The external jitter is computed from the overall and internal jitter. The signal-to-noise ratio of the data converter (102) is computed from the external jitter.

**22 Claims, 3 Drawing Sheets**



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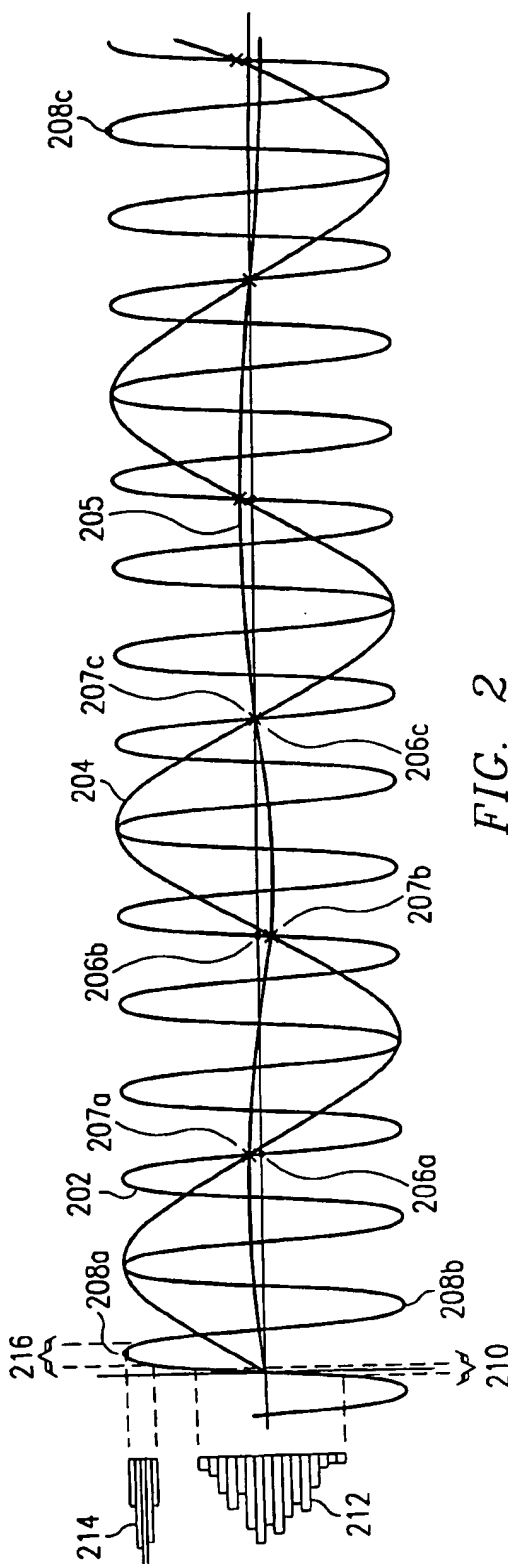
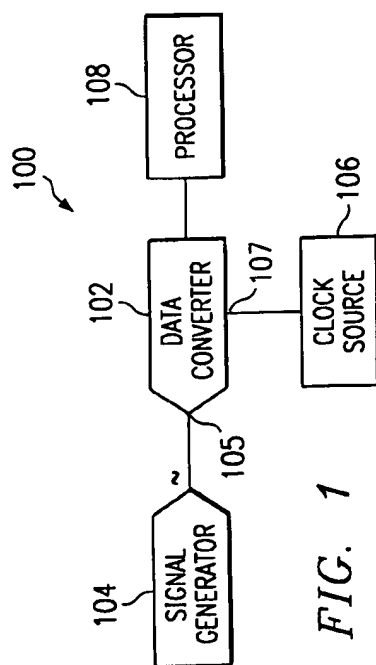
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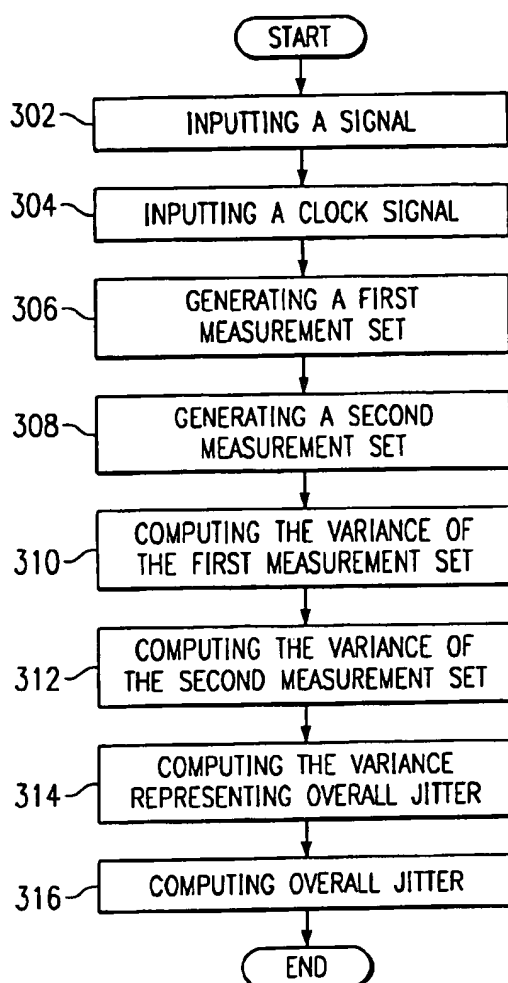


FIG. 3

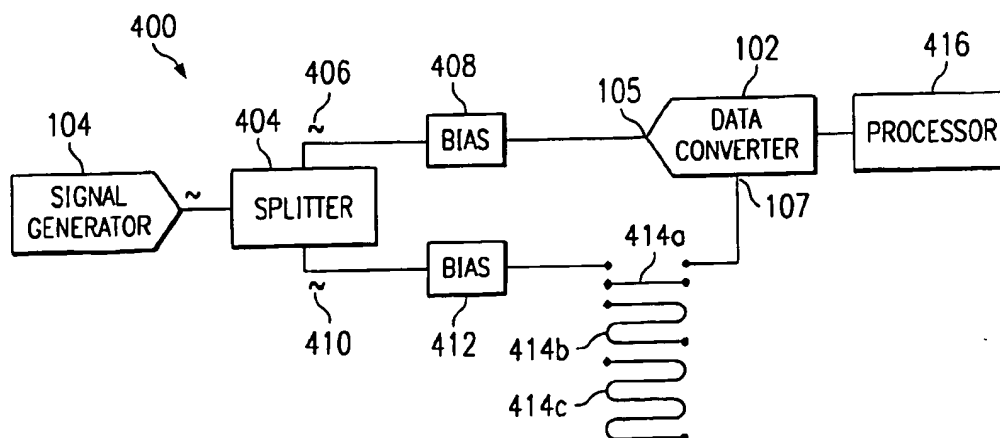
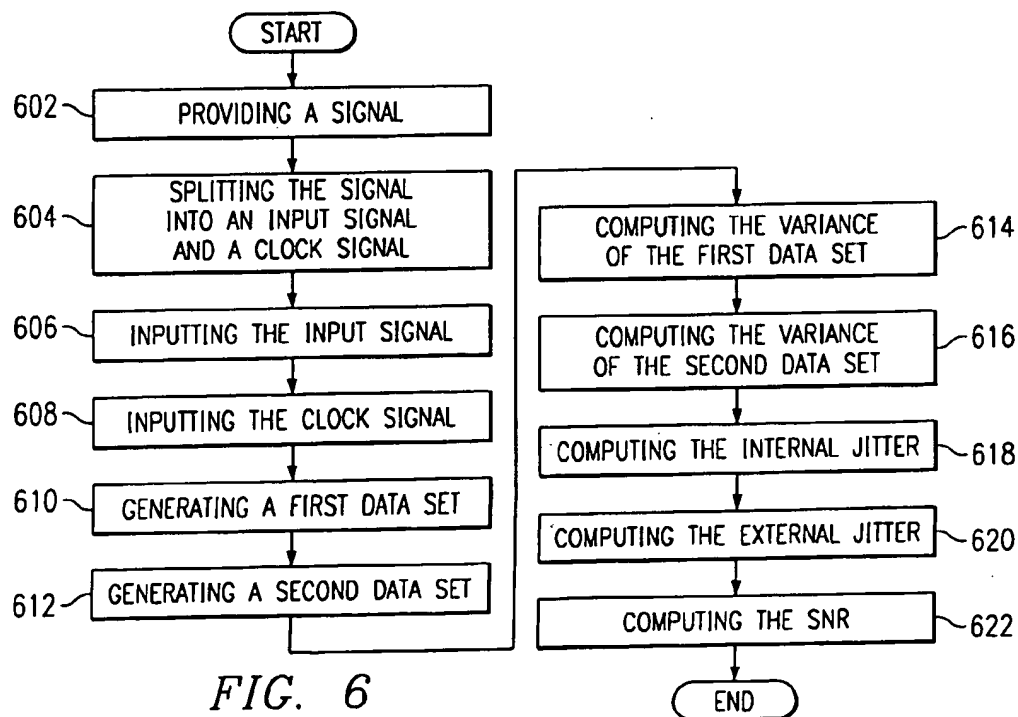
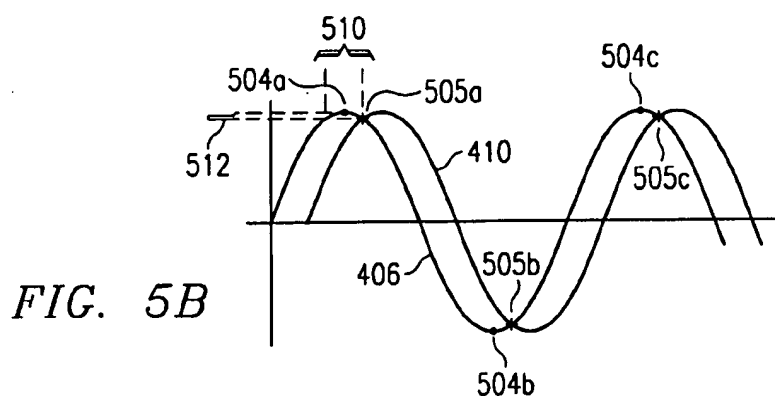
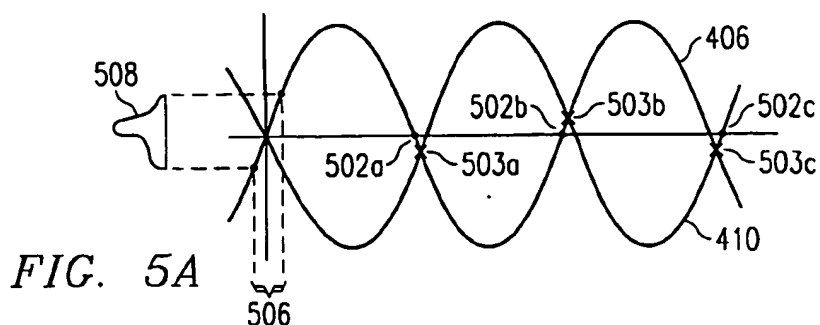


FIG. 4



# METHOD AND SYSTEM FOR MEASURING JITTER

This application claims priority under 35 USC §119(e) (1) of provisional application No. 60/171,260 filed Dec. 15, 1999.

## TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of electronic circuits and more specifically to a method and system for measuring jitter.

## BACKGROUND OF THE INVENTION

The growing use of data converters has created a demand for more accurate and more precise methods for measuring jitter. Sampling time noise, or jitter, is a component of signal-to-noise ratio (SNR), which is an important parameter in assessing the performance of a data converter. Jitter causes deviations in the sampling time, which in turn causes deviations in the value of the signal sample. Jitter becomes a major factor in the SNR at relatively high input frequencies, for example, the frequencies at which communications analog-to-digital converters (ADCs) operate, because even a small deviation in the sampling time may result in a large deviation in the value of the signal sample. As the demand for intermediate frequency sampling in communication systems increases, ADC manufacturers are faced with the task of measuring the SNR at very high input frequencies. The SNR at high input frequencies may be measured using a test system with very low jitter. Even state-of-the-art test systems, however, cannot meet the low jitter requirement. Alternatively, the SNR may be measured using test systems with medium jitter by measuring the jitter of the system and then calibrating out the jitter. Known methods and systems of measuring jitter, however, have not been completely satisfactory in terms of accuracy, precision, and speed.

Calculation of the maximum jitter tolerance for a data converter begins with computing the SNR. Theoretically, the best possible SNR of an N-bit converter, assuming that the input is uniformly distributed between two adjacent data converter codes, is given by Equation (1):

$$SNR_{max}(dBs) = 6.02N - 6N \quad (1)$$

Practically, the measured SNR of a data converter may be worse than the above prediction due to various factors, including jitter. Overall jitter may be due to internal factors inside of the data converter such as the aperture jitter of a sample and hold circuit or to external factors such as the jitter of a clock source or the phase noise of an input wave generator. If the amplitude noise due to overall jitter is integrated and the input is a sine wave, Equation (2) describes how overall jitter limits the best SNE of a data converter:

$$SNR_{max}(dBs) = 20 \log(2n\epsilon) \quad (2)$$

where f is the input frequency, and  $\epsilon$  is the root mean square (rms) value of the overall jitter in the system. Assuming that the jitter induced noise level should be less than the quantization noise of an ideal converter, Equations (1) and (2) may be equated to yield Equation (3) describing the maximum jitter tolerance of a data converter:

$$\epsilon < \frac{1}{f \cdot 10^{0.3N} \cdot 2\pi} \quad (3)$$

According to Equation (3), less than 1 ps rms jitter is tolerated in a 14-bit communication ADC sampling a 70 MHz if signal. This requirement is very stringent considering the fact that the typical jitter found in CMOS digital logic circuits is around 20–30 ps rms. Other maximum jitter tolerance levels are shown in TABLE 1.

TABLE 1

Maximum Jitter Tolerance for ADCs (ps rms $\times$ 2 $\pi$ )					
Bits	8	10	12	14	16
Input Frequency:					
10 KHz	398107	100000	10000	6309	1585
100 KHz	39810	10000	1000	631	158
1 MHz	3981	1000	100	63	15.8
10 MHz	398	100	10	6.3	1.58
100 MHz	40	10	1	0.63	0.16

The stringent low jitter requirement makes the measurement of the SNR of data converters extremely difficult. According to a known approach for measuring the SNR, the SNR is directly measured. This approach requires that the jitter of the system used to measure the SNR of the data converter be much lower than the maximum jitter tolerance level. Low jitter sine wave generators and clock sources, however, are very expensive and often fail to meet the performance requirements needed to measure the SNR of communication ADCs. Moreover, it is difficult to integrate low jitter sine wave generators and clock sources into production testers. In another approach for measuring the SNR, instead of using an ideal clock source or sine wave generator to minimize system jitter, the noise due to system jitter is measured and calibrated out from the overall noise. Such calibration techniques, however, remove the requirement for low jitter hardware at the expense of the need for accurate and precise jitter measurements. For such calibration to work, the accuracy of the jitter measurement has to be much better than the jitter in the test system.

Known methods of measuring jitter include the sampling scope methods, comparator methods, and phase noise methods. According to the sampling scope methods, a clock waveform is digitized at a high speed and the time between the two signals edges is measured. Jitter is computed from the standard deviation of the measurements. A disadvantage of these methods is that the scope timebase must be jitter-free. Moreover, the accuracy of these methods is limited to approximately 10 ps rms, partly due to the insufficient 8-bit resolution of the ADCs used in scopes. The comparator methods use a comparator to trigger at the zero crossings of the clock and start a coarse and a fine counter. The fine counter works by digitizing the discharge voltage of a capacitor. The coarse counter takes the average of multiple measurements of the time between the zero crossings. These methods, however, are slow. Moreover, the accuracy of these methods is limited to approximately 10 ps rms. The phase noise methods measure the phase noise and mathematically relate the phase noise to clock jitter. These methods, however, require a very low phase noise signal generator and a high quality mixer to mix down the fundamental components of the clock frequency to the base band. Moreover, these methods are frequency-based and are very slow.

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While these approaches have provided improvements over prior approaches, the challenges in the field of electronic circuits have continued to increase with demands for more and better jitter measurement techniques having greater accuracy and precision. Therefore, a need has arisen for a new method and system for measuring jitter.

### SUMMARY OF THE INVENTION

In accordance with the present invention, a method and system for measuring jitter are provided that substantially eliminate or reduce the disadvantages and problems associated with previously developed systems and methods.

According to one embodiment of the present invention, a system for measuring overall jitter is disclosed that comprises a data converter and a signal generator. The signal generator is coupled to the data converter and outputs a signal to the data converter. The data converter measures the signal to generate a first measurement set representing overall jitter and system noise, and to generate a second measurement set representing system noise. The overall jitter is computed using the first measurement set and the second measurement set. More specifically, the overall jitter is computed using the variance of the first measurement set and the variance of the second measurement set.

According to one embodiment of the present invention, a method for measuring overall jitter is disclosed. First, a signal is input into a data converter. Second, a first measurement set representing overall jitter and system noise is generated by measuring the signal. Third, a second measurement set representing system noise is generated by measuring the signal. Finally, the overall jitter is computed using the first measurement set and the second measurement set. More specifically, the overall jitter is computed using the variance of the first measurement set and the variance of the second measurement set.

According to one embodiment of the present invention, a system for measuring internal jitter is disclosed that comprises a signal generator that generates a signal. A splitter coupled to the signal generator splits the signal into an input signal and a clock signal. A data converter coupled to the splitter measures the input signal using the clock signal to generate a first data set representing internal jitter and system noise and to generate a second data set representing system noise. The internal jitter is computable using the first data set and the second data set. More specifically, the internal jitter is computed using the variance of the first data set and the variance of the second data set.

According to one embodiment of the present invention, a method for measuring internal jitter is disclosed. First, a signal is provided. Second, the signal is split into an input signal and a clock signal. Third, the input signal is input into a data converter. Fourth, the clock signal is input into the data converter. Fifth, a first data set representing internal jitter and system noise is generated by measuring the input signal using the data converter. Sixth, a second data set representing system noise is generated by measuring the input signal using the data converter. Finally, the internal jitter is computed using the first data set and the second data set. More specifically, the internal jitter is computed using the variance of the first data set and the variance of the second data set.

A technical advantage of the present invention is that, unlike the measurements of known approaches, the calculation of overall jitter and internal jitter does not include system noise, resulting in a more accurate estimate of jitter, approximately 0.1 ps rms accuracy. The exclusion of system

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noise also results in more accurate estimate of signal-to-noise ratio. Another technical advantage of the present invention is that the external jitter may be determined using the internal and overall jitter, allowing for a measurement of the jitter of the test system. Another technical advantage of the present invention is that it does not require practically jitterless components to determine the overall jitter and internal jitter of a data converter. Practically jitterless components are often expensive and fail to meet the requirements needed to measure the jitter of a communications data converter. Therefore, the present invention allows for a more accessible, more accurate calculation of jitter. Other technical advantages are readily apparent to one of skill in the art.

### BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and for further features and advantages, reference is now made to the following description, taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of one embodiment of a system for measuring overall jitter that may be used in accordance with the present invention;

FIG. 2 is a graph illustrating a first measurement set and a second measurement set generated in one embodiment of a method for measuring overall jitter in accordance with the present invention;

FIG. 3 is a flowchart demonstrating one embodiment of a method for measuring overall jitter in accordance with the present invention;

FIG. 4 is a block diagram of one embodiment of a system for measuring internal jitter that may be used in accordance with the present invention;

FIG. 5A is a graph illustrating a first data set generated in one embodiment of a method for measuring internal jitter in accordance with the present invention;

FIG. 5B is a graph illustrating a second data set generated in one embodiment of a method for measuring internal jitter in accordance with the present invention; and

FIG. 6 is a flowchart demonstrating one embodiment of a method for measuring internal jitter in accordance with the present invention.

### DETAILED DESCRIPTION OF THE DRAWINGS

Various embodiments of the present invention and its advantages are best understood by referring to FIGS. 1-6 of the drawings, like numerals being used for like and corresponding parts of the various drawings.

FIG. 1 is a block diagram of one embodiment of a system 100 for measuring overall jitter that may be used in accordance with the present invention. The system 100 comprises a data converter 102, and a signal generator 104, a clock source 106, and a processor 108, all of which may be coupled to the data converter 102. The overall jitter of the system 100 includes the internal jitter of the data converter 102, the signal generator 104, and the clock source 106. The data converter 102 may be, for example, a high-frequency, high-amplitude, high-SNR analog-to-digital converter (ADC), for example, a ten- to sixteen-bit communication ADC. Time jitter creates a large variation in the output of the data converter 102 when the input has a high frequency and a high amplitude. Thus, a high-frequency, high-amplitude input may be used to improve sensitivity to jitter. Undersampling may be also used to achieve a desired jitter sensitivity. Undersampling occurs when the frequency of an input signal is greater than one-half the sampling frequency.

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By using undersampling, the input frequency may be high, while the sampling frequency does not have to be high. Additionally, a converter with a high SNR may also be used to improve jitter sensitivity. For these reasons, ten- to sixteen-bit communication ADCs may provide more jitter sensitivity than the eight-bit ADCs often used in scopes.

The signal generator 104 may be, for example, a low phase noise sine wave generator or square wave generator. The signal generator 104 may be operable to output to the data converter 102 a signal that has maximum slew rate points, points of greatest slope, and minimum slew rate points, points of zero slope. The clock source 106 may be synchronized with the signal generator 104, for example, it may be phase locked with the signal generator 104. The signal from the signal generator 104 may be sent to the input 105 of the data converter 102, and may be used as the signal to be sampled. The signal from the clock source 106 may be sent to the clock 107 of the data converter 102, and may be used to determine which points of the input signal are to be sampled. If the input source has very low jitter, the clock source 106 may be the main source of the jitter. The processor 108 may be used to compute the overall jitter from the output of the data converter 102.

In general, the data converter 102 is operable to generate a first measurement set by sampling the signal at the maximum slew rate points of the signal, and is operable to generate a second measurement set by sampling the signal at the minimum slew rate points of the signal. The overall jitter may then be computed using the first and the second measurement sets.

FIG. 2 is a graph illustrating a first measurement set and a second measurement set generated in one embodiment of a method for measuring overall jitter in accordance with the present invention. A signal 202 may be an output from the signal generator 104, and a clock signal 204 may be an output from the clock source 106. The output signal 205 from the data converter 102 is formed by the sampling of the signal 202 by the clock signal 204. Note that the output signal 205 may be a sine wave. In this embodiment, the signal 202 and the clock and signal 204 are sine waves. The signal 202 has maximum slew rate points 206a, 206b and 206c, which are the points of greatest slope of the sine wave. The signal 202 also has minimum slew rate points 208a, 208b, and 208c, which are points of zero slope of the sine wave. The signal generator 104 and the clock source 106 may be synchronized, and may be, for example, phase-locked. The frequency of the clock signal 204 may be less than that of the signal 202. To capture a clear sine wave, the frequency of the signal 202 may be slightly larger than the frequency of the clock signal 204 multiplied by an integer. For example, the frequency of the clock signal 204 may be approximately 20 MHz, and the frequency of the signal 202 may be slightly larger than 100 MHz.

The overall jitter and the system noise cause the clock signal 204 and the signal 202 to fluctuate such that an attempted sampling of the maximum slew rate points 206a-c may result in actually sampling points 207a-c within a range 210 around the maximum slew rate points 206a-c. Since the slope is large around the maximum slew rate points 206a-c, deviations from the maximum slew rate points 206a-c cause a large variance in the measurements of the sine wave. Note that undersampling may be used to achieve a high slew rate. Undersampling occurs when frequency of an input signal is greater than one-half the sampling frequency. By using undersampling, the input frequency may be increased, thus increasing the slew rate, without increasing the sampling rate. A first measurement

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set 212 describes the measurements of the signal 202 at points sampled from within the range 210, and represents overall jitter and system noise.

In order to calculate overall jitter without system noise, the second measurement set 214 is generated by measuring the signal 202 at minimum slew rate points 208a-c. System noise, but not jitter, causes the deviations when sampling the minimum slew rate points 208a-c, resulting in a range 216 of sampled points. The deviations caused by the system noise result in a variance of the measurements of the minimum slew rate points 208a-c, which are represented by the second measurement set 214. The overall jitter may be computed from the variances of the first measurement set 212 and the second measurement set 214. The variances may be computed using any suitable method, for example, directly from the measurements, using histograms, or using fast Fourier transforms.

FIG. 3 is a flowchart demonstrating one embodiment of a method for measuring overall jitter in accordance with the present invention. In general, the method shown inputs the signal 202 and the clock signal 204 into the data converter 102. Using the clock signal 204, the data converter measures the signal 202 at the maximum slew rate points 206a-c to formulate the first measurement set 212 representing overall jitter and system noise. The data converter 102 measures the signal 202 at the minimum slew rate points 208a-c to formulate the second measurement set 214 representing system noise. The overall jitter is computed from the first measurement set 212 and the second measurement set 214.

Specifically, the method begins with step 302, where the signal 202 is input into the input 105 of the data converter 102. The signal 202 may be, for example, a sine wave signal generated by a sine wave generator. The signal 202 and the clock signal 204 may be synchronized with each other, and they may be, for example, phase-locked with each other. The frequency of the clock signal 204 may be less than that of the signal 202. For example, the frequency of the clock signal 204 may be approximately 20 MHz, and the frequency of the signal 204 may be approximately 100 MHz. In step 304, the clock signal 204 generated by the clock source 106 is sent to the clock 107 of the data converter 102.

The method then moves to step 306, where the first measurement set 212 representing overall jitter and system noise is generated. When attempting to sample the maximum slew rate points 206a-c, the overall jitter and system noise cause the clock signal 204 and the signal 202 to fluctuate and sample points within the range 210 around the maximum slew rate points 206a-c. Since the slope at the maximum slew rate points 206a-c is large, deviations around these points result in a large variance of the measurements of the signal 202. The variance of first measurement set 212 of the measurements around the maximum slew rate points 206a-c corresponds to the sum of the square of the system noise and the square of the overall jitter induced noise, from which the overall jitter and system noise can be computed. The variance may be computed from a histogram of the first measurement set 212, where the histogram is normalized to form  $H_{max}(x)$ . In step 308, the second measurement set 214 representing system noise is generated. System noise, but not overall jitter, causes deviations 216 when sampling of the minimum slew rate points 208a-c, resulting in a variance of the measurements of the signal 202. The variance of the second measurement set 214 of the measurements around the minimum (zero) slew rate points 208 corresponds to the square of the system noise. The variance may be computed from a histogram of the second measurement set 214, where the histogram is normalized to form  $H_{min}(x)$ .



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In general, in steps 310–316, the overall jitter is computed from the variance of the normalized first histogram  $H_{max}(x)$  and the variance of the normalized second histogram  $H_{min}(x)$ . Specifically, in step 310, the variance of  $H_{max}(x)$  generated in step 306 may be computed either directly from the data set or by using Equation (4):

$$var_1 = \int (x - \bar{x}_1)^2 H_{max}(x) dx \quad (4)$$

where

$$\bar{x}_1 = \int x H_{max}(x) dx$$

In step 312, the variance of  $H_{min}(x)$  generated in step 308 may be computed either directly from the data set or by using Equation (5):

$$var_2 = \int (x - \bar{x}_2)^2 H_{min}(x) dx \quad (5)$$

where

$$\bar{x}_2 = \int x H_{min}(x) dx$$

The variances of the first measurement set 212 and the second measurement set 214 may be computed using another suitable method, for example, computed directly from the measurement sets 212 and 214 or using fast Fourier transforms.

In step 314, the variance representing overall jitter is obtained by subtracting the variance representing system noise from the variance representing overall jitter and system noise, as shown by Equation (6):

$$var_j = var_1 - var_2 \quad (6)$$

In step 316, the overall jitter is computed from the variance representing overall jitter, as shown in Equation (7):

$$j_{overall} = \frac{1}{2\pi Af} \sqrt{var_j} \quad (7)$$

After computing the overall jitter, the method terminates.

FIG. 4 is a block diagram of one embodiment of a system 400 for measuring internal jitter that may be used in accordance with the present invention. In general, the system 400 comprises a signal generator 104 coupled to a splitter 404 coupled to the data converter 102. Specifically, the signal generator 104 may be, for example, a low phase noise sine wave generator. The splitter 404, which may be, for example, a power splitter, splits the signal from the signal generator 104 into a splitter-input signal 406 and a splitter-clock signal 410. A splitter-input signal 406 of the splitter 404 may be biased using a first bias circuit 408 coupled to the splitter 404 and the data converter 102. The splitter-input signal 406 may be sent to the input 105 of the data converter 102. A splitter-clock signal 410 of the splitter 404 may be biased using a second bias circuit 412 coupled to the splitter 404 and the data converter 102. The splitter clock signal 410 may be sent to the clock 107 of the data converter 102. Since the signals to the input 105 and the clock 107 of the data converter are from the same source, any jitter in the source signal is present at both the clock and the input, canceling the jitter of the input and clock signals. The internal noise of the data converter 102 may be canceled by repeating the measurements under different phase conditions between the input and the clock, which may be obtained by varying the length of either the splitter-input signal 406 path or the splitter-clock signal 410 path. These paths may be varied by,

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for example, using traces 414a–c of different lengths, using relays to switch between the traces. A processor 416 may be used to compute the internal jitter of the data converter 102.

In general, when the clock and input frequencies are the same, the input is undersampled at twice the Nyquist frequency. If there were no noise or jitter, the output would be a straight direct current line at certain codes of the data converter. When jitter or noise is present, they can be measured from the data at the maximum and minimum slew rate points of the input signal. The data converter 102 is operable to generate a first data set by sampling the input signal at the maximum slew rate points of the input signal, and is operable to generate a second data set by sampling the input signal at the minimum slew rate points of the input signal. The internal jitter may then be computed from the first and the second data sets.

FIG. 5A is a graph illustrating a first data set generated in one embodiment of a method for measuring internal jitter in accordance with the present invention. The splitter-input signal 406 has maximum slew rate points 502a–c, which are the points of maximum slope of the splitter-input signal 406. Maximum slew rate points 502a–c are sampled by capturing data around the mid-code of the data converter 102. When attempting to sample the maximum slew rate points 502a–c, internal jitter and system noise cause the data converter 102 to fluctuate and to sample points 503a–c in a range 506 around the maximum slew rate points 502a–c, resulting in a variance in the measurements of the splitter-input signal 406. The variance of the first data set 508 of measurements of the points sampled around the maximum slew rate points 502 represents internal jitter and the data converter's 102 random noise.

FIG. 5B is a graph illustrating a second data set generated in one embodiment of a method for measuring internal jitter in accordance with the present invention. The splitter-input signal 406 has minimum slew rate points 504a–c, which are the points of zero slope of the splitter-input signal 406. Minimum slew rate points 504a–c are sampled by capturing data around the zero-scale or full-scale codes of the data converter 102. System noise causes the data converter 102 to fluctuate when sampling the minimum slew rate points 504a–c and measure points 505a–c within a range 510 around the points 504a–c, resulting in a variance of measurements. The variance of the second data set 512 of measurements of points sampled around the minimum slew rate points 504a–c represents the system noise.

FIG. 6 is a flow chart demonstrating one embodiment of a method for measuring internal jitter in accordance with the present invention. In general, in this embodiment, the splitter 404 splits a signal, for example, a radio frequency signal, into a splitter-input signal 406 that is sent to the input 105 of the data converter 102, and splitter-clock signal 410 that is sent to the clock 107 of the data converter 102. The data converter 102 samples the maximum slew rate points 502a–c of the splitter-input signal 406 to generate the first data set 508 representing internal jitter and system noise. The data converter 102 samples the minimum slew rate points 510 of the input signal 406 in order to generate the second data set 512 representing system noise. The internal jitter is computed from the first data set 508 and the second data set 512. The external jitter is computed from the overall jitter and the internal jitter. Finally, the signal-to-noise-ratio (SNR) is computed from the external jitter.

Specifically, the method begins with step 602, where a signal is provided. The signal may be provided using, for example, using the signal generator 402. In step 604, the signal is split using the splitter 404 into the splitter-input

signal 406 and the splitter-clock signal 410. The input signal has maximum slew rate points 502a-c and minimum slew rate points 504a-c. In step 606, the splitter-input signal 406 is input into the input 105 of the data converter 102. In step 608, the clock signal 410 is input into the clock 107 of the data converter 102.

The method proceeds to step 610, where the first data set 508 is generated. When attempting to sample the maximum slew rate points 502a-c, internal jitter and system noise cause the data converter 102 to sample points in the range 506 around the points 502a-c, which causes a variance in the measurements of the splitter-input signal 406. The variance of the histogram of the first data set 508 of measurements around the maximum slew rate points represents internal jitter and system noise. To measure the maximum slew rate points 502a-c, the path lengths of the splitter input 406 and the splitter-clock 410 signals are varied until the measured data is around the mid-scale code of the data converter 102. In step 612, the second data set 512 is generated. System noise causes deviations when sampling the minimum slew rate points 504a-c, which results in a variance in the measurements of the splitter-input signal 406 around the minimum slew rate points 504a-c. The variance of the histogram of the second data set 512 of measurements represents system noise. To sample the minimum slew rate points 504a-c, the path lengths of the splitter input 406 and the splitter-clock 410 signals may be varied, for example, using traces 414a-c, until the measured data is around the zero-scale or full-scale codes of the data converter 102.

In general, in steps 614 through 618, the internal jitter is calculated from the variance of the first data set 508 generated in step 610 and the variance of the second data set 512 generated in step 612. Specifically, in step 614, the variance  $\text{var}_1$  of the first data set 508 is computed. The variance may be computed, for example, by directly computing the variance from the data. Other appropriate alternatives may be used, for example, computing the variance from a histogram or a Fourier transform of the data set. In step 616, the variance  $\text{var}_2$  of the second data set 512 is computed. As in step 614, variance  $\text{var}_2$  may be computed, for example, directly from the data or from a histogram or a Fourier transform of the data set.

In step 618, the internal jitter is computed using Equation (8):

$$j_{\text{internal}} = \frac{1}{2\pi} \sqrt{\frac{\text{var}_1 - \text{var}_2}{[(f_1 A_1 \cos(\theta_1))^2 - (f_2 A_2 \cos(\theta_2))^2]}} \quad (8)$$

$f_1$  is the frequency of the signal of the first data set;

$f_2$  is the frequency of the signal of the second data set;

$A_1$  is the amplitude of the signal of the first data set;

$A_2$  is the amplitude of the signal of the second data set;

$\text{output}_1$  is the average value of the measured outputs from the first data set;

$\text{output}_2$  is the average value of the measured outputs from the second data set.

$$\theta_1 = \arcsin\left(\frac{2 \cdot \text{output}_1}{A_1}\right); \text{ and}$$

$$\theta_2 = \arcsin\left(\frac{2 \cdot \text{output}_2}{A_2}\right)$$

Note that the measurements may be taken such that  $f_1=f_2$  and  $A_1=A_2$ , and the path lengths for the splitter clock 406 and the

splitter input 410 signals are different. Note also that any amplitude, frequency or phase may be used in the above formulas.

The accuracy of the measurement depends on the size of the following value:

$$[(f_1 A_1 \cos(\theta_1))^2 - (f_2 A_2 \cos(\theta_2))^2]$$

If the value is sufficiently large, the measurement will be more accurate. While known approaches have an accuracy of approximately 10 ps rms, this embodiment of the method of measuring jitter has an accuracy of approximately 0.1 ps rms.

In step 620, the external jitter is calculated from the internal jitter determined in step 614 and the overall jitter. Assuming no correlation between the noise sources, the external jitter is given by Equation (9):

$$j_{\text{external}} = \sqrt{j_{\text{overall}}^2 - j_{\text{internal}}^2} \quad (9)$$

Also, the external jitter induced noise is given by Equation (10):

$$n_{j,\text{external}} = \sqrt{2} A f j_{\text{external}} \quad (10)$$

where 'A' is the input amplitude and 'f' is the input frequency.

Finally, in step 622, the SNR is calculated from the external jitter from step 620. The SNR is calculated by calibrating out the effects of the external jitter. The true SNR of the data converter 102 is given by Equation (11):

$$\text{SNR}_{\text{true}} = 10 \log \left( \frac{A^2 / 2}{N^2 - n_{j,\text{external}}^2} \right) \quad (11)$$

While a known method may estimate the SNR of a 12 bit 66 MSPS communication ADC at a frequency of 16 MHz to be approximately 58 dBs, applying the method of jitter correction to the calculation of the SNR of the same ADC may yield an SNR value of approximately 63 dBs.

A technical advantage of the present invention is that, unlike the measurements of known approaches, the calculation of overall jitter and internal jitter does not include system noise, resulting in a more accurate assessment of jitter, approximately 0.1 ps rms accuracy. The exclusion of system noise also results in more accurate assessment of signal-to-noise ratio. Another technical advantage of the present invention is that it does not require jitterless components to determine the overall jitter and internal jitter of a data converter. Practically jitterless components are often expensive and fail to meet the requirements needed to measure the jitter of a communications data converter. Therefore, the present invention allows for a more accessible, more accurate calculation of jitter, resulting in a more accurate test of a data converter.

Although an embodiment of the invention and its advantages are described in detail, a person skilled in the art could make various alternations, additions, and omissions without departing from the spirit and scope of the present invention as defined by the appended claims.

What is claimed is:

1. A system for measuring jitter, the system comprising:
  - a signal generator operable to output a signal;
  - a data converter coupled to the signal generator, and operable to periodically measure the signal near maximum slew rate points of the signal to generate a first measurement set and to periodically measure the signal

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near minimum slew rate points of the signal to generate a second measurement set; and  
 circuitry coupled to the data converter, for computing a measurement of jitter using the first measurement set and the second measurement set.

2. The system of claim 1 wherein the data converter is an analog-to-digital converter.

3. The system of claim 1 wherein the signal generator is a sine wave generator.

4. The system of claim 1 wherein the signal generator is a square wave generator.

5. The system of claim 1 further comprising a clock source coupled to the data converter, wherein the clock source is operable to output a clock signal to the data converter and is synchronized with the signal generator.

6. The system of claim 1 further comprising a clock source coupled to the data converter, wherein the clock source is operable to output a clock signal to the data converter and is phase locked with the signal generator.

7. The system of claim 1 wherein:  
 the variance of the first measurement set represents overall jitter and system noise;  
 the variance of the second measurement set represents system noise; and  
 the overall jitter is computable using the variance of the second measurement set and the variance of the first measurement set.

8. A method for measuring jitter, the method comprising:  
 inputting a signal into a data converter;  
 generating a first measurement set by periodically measuring the signal near its maximum slew rate points using the data converter;  
 generating a second measurement set by periodically measuring the signal near its minimum slew rate points using the data converter; and  
 computing the jitter using the first measurement set and the second measurement set.

9. The method of claim 8 wherein the data converter is an analog-to-digital converter.

10. The method of claim 8 wherein the signal is a sine wave.

11. The method of claim 8 further comprising inputting a clock signal into the data converter, wherein the clock signal is synchronized with the signal.

12. The method of claim 8 further comprising inputting a clock signal into the data converter, wherein the clock signal is phase-locked with the signal.

13. The method of claim 8 wherein the step of computing comprises:  
 computing the variance of the first measurement set, wherein the variance of the first measurement set represents overall jitter and system noise;  
 computing the variance of the second measurement set, wherein the variance of the second measurement set represents system noise; and  
 computing the overall jitter using the variance of the second measurement set and the variance of the first measurement set.

14. The method of claim 8 wherein the step of computing comprises:  
 computing the variance of the first measurement set using a first histogram of the first measurement set, wherein the variance of the first measurement set represents overall jitter and system noise;  
 computing the variance of the second measurement set using a second histogram of the second measurement

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set, wherein the variance of the second measurement set represents system noise; and  
 computing the overall jitter using the variance of the second measurement set and the variance of the first measurement set.

15. The method of claim 8 wherein the step of computing comprises:  
 computing the variance of the first measurement set using a Fourier transform of the first measurement set, wherein the variance of the first measurement set represents overall jitter and system noise;  
 computing the variance of the second measurement set using a Fourier transform of the second measurement set, wherein the variance of the second measurement set represents system noise; and  
 computing the overall jitter using the variance of the second measurement set and the variance of the first measurement set.

16. A system for measuring jitter, the system comprising:  
 a signal generator operable to generate a signal;  
 a splitter coupled to the signal generator and operable to split the signal into an input signal and a clock signal;  
 a data converter coupled to the splitter and operable to periodically measure the input signal near its maximum slew rate points using the clock signal to generate a first data set and to periodically measure the input signal using the clock signal near its minimum slew rate points to generate a second data set; and  
 circuitry, coupled to the data converter, for computing the jitter using the first data set and the second data set.

17. The system of claim 11 wherein the data converter is an analog-to-digital converter.

18. The system of claim 11 wherein the signal generator is a sine wave generator.

19. The system of claim 11 wherein the signal generator is a square wave generator.

20. The system of claim 16 wherein:  
 the variance of the first data set represents internal jitter and system noise;  
 the variance of the second data set represents system noise; and  
 the internal jitter is computable using the variance of the second data set and the variance of the first data set.

21. A method for measuring external jitter, the method comprising:  
 measuring the overall jitter by:  
 inputting a signal into a data converter;  
 generating a first measurement set representing overall jitter and system noise by measuring the signal using the data converter;  
 generating a second measurement set representing system noise by measuring the signal using the data converter; and  
 computing the overall jitter using the first measurement set and the second measurement set;  
 measuring the internal jitter by:  
 providing a signal;  
 splitting the signal into an input signal and a clock signal;  
 inputting the input signal into a data converter;  
 providing the clock signal into the data converter;  
 generating a first data set representing internal jitter and system noise;  
 generating a second data set representing system noise; and

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computing the external jitter using the first data set and the second data set; and

calculating the external jitter using the overall jitter and the internal jitter.

22. A method for measuring signal-to-noise ratio, the method comprising:

measuring the overall jitter by:

inputting a signal into a data converter;

generating a first measurement set representing overall jitter and system noise by measuring the signal using the data converter;

generating a second measurement set representing system noise by measuring the signal using the data converter; and

computing the overall jitter using the first measurement set and the second measurement set;

measuring the internal jitter by:

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providing a signal;

splitting the signal into an input signal and a clock signal;

inputting the input signal into a data converter;

providing the clock signal into the data converter;

generating a first data set representing internal jitter and system noise;

generating a second data set representing system noise; and

computing the external jitter using the first data set and the second data set;

calculating the external jitter using the overall jitter and the internal jitter; and

calculating the signal-to-noise ratio using the external jitter.

\* \* \* \* \*

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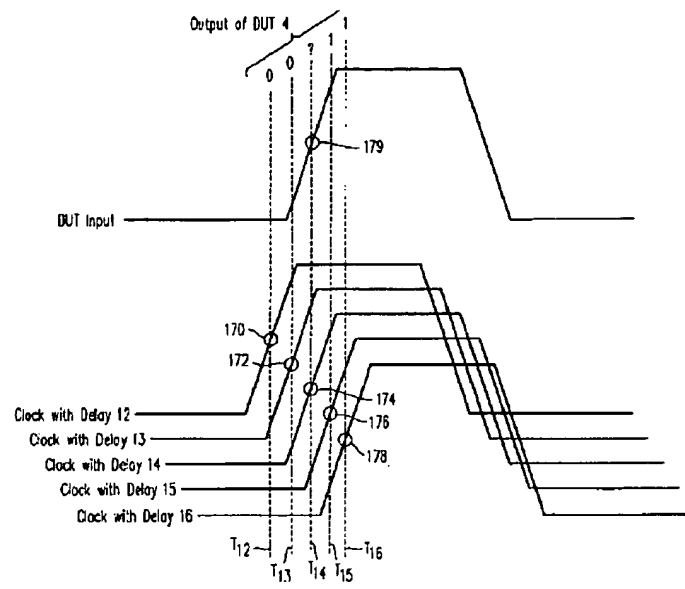


FIG. 8